



Final Report

# INTEGRATED THIN-FILM CADMIUM SULFIDE SOLAR CELL MODULE

by

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THE BOEING COMPANY

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16. Abstract The development of flexible, integrated thin-film Cds solar cells and modules by utilizing integrated electronic circuit technology is described. The experimental developments discussed in this final report are mostly related to single cells fabricated in 3-cell submodule structures. Cell structures are formed with vacuum-deposited films onto 1-mil kapton.  Ohmic contact and high adherence to the Cds films is achieved with chromium thin films. SiOx films are used to increase the rigidity of the kapton. Barrier layers are formed using both the conventional process of immersion in a CuCl solution and a vacuum deposition or dry process. The dry process is shown to be superior. Cell segments with vacuum-deposited grids exhibit open-circuit voltages of 510 mv, short circuit current densities of 11.8 mA/cm <sup>2</sup> , and efficiencies of 2.7 percent when tested under AMO conditions and at a temperature of 25°C.					
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## FOREWORD

This final report describes the work done on a 2-year research program conducted by The Boeing Company, Engineering and Research Division, under NASA Contract NAS 3-13232. Emphasis is placed on the second year's development work. The work described herein was accomplished under the management of the NASA Project Manager, Mr. F. J. Stenger and later Mr. A. F. Ratajczak, Direct Energy Conversion Division, NASA-Lewis Research Center.



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## SUMMARY

This report describes the 2 years of activity on a program to design, develop, fabricate, and test flexible integrated thin-film cadmium sulfide solar cells and modules.

The program was oriented towards developing low-cost and high-production-rate methods for interconnecting cells into very large solar arrays. The initial activity was concerned only with developing single cells. During later activity, a 3-cell submodule was developed that provided more cells per deposition sequence and also development of interconnect techniques.

Deposition masks were fabricated that allow the cell structures and interconnects to be constructed by through-mask vacuum deposition techniques. Vacuum-metallized kapton film was used as substrates for the single cells and for the 3-cell submodules. A deposition fixture was designed and fabricated to position the substrates and manipulate the desired masks and vapor source materials necessary to form the cells.

A nichrome thin film was used to achieve high film adherence to the kapton layer. The nichrome was followed by a 1 to 2 micron copper film to form the main cell metallization. Chromium thin films were applied extensively in the deposited cell structures as a means to: (1) achieve high adherence between the CdS films and the vacuum-metallized copper substrates; (2) obtain an ohmic contact to the CdS films; and (3) improve the adherence of the gold films as grids or contact areas.

Both the conventional wet CuCl chemical exchange process and a dry (vacuum deposition) process were considered for formation of the  $\text{Cu}_2\text{S}$  barrier layer. While the wet CuCl method was investigated during the early part of the program, emphasis towards the end of the contract was on the fabrication of cells by means of a dry barrier formation. Vacuum-deposited  $\text{SiO}_x$  films were used originally to mask the CdS film edges during immersion for a prebarrier etch and wet barrier formation but a silk screened silicone, Dow-Corning Sylgard 186, was later shown to give substantially better edge protection.  $\text{SiO}_x$  deposited prior to any cell layer on the back surface of the kapton substrate was used to produce nearly flat cell structures following the thick CdS deposition.

Using advanced mask fabrication techniques, grid masks were developed that resulted in 2 mil-wide lines on 20-mil centers. Deposited gold grid films up to 0.5-micron thick were obtained with these masks.

Measurements on device performance were made under AMO conditions at both 25°C and 60°C, with the majority of the measurements at the lower temperature. Dry processed cell segments have yielded performance parameters of the following: open-circuit voltage of 510 mv, short-circuit-current density of 11.8 mA/cm<sup>2</sup> with a fill factor of 63.8 percent and a conversion efficiency of 2.7 percent.

## INTRODUCTION

This document reports the results of a developmental program on an Integrated Thin-Film Cadmium Sulfide Solar Cell Module. The program was conducted by The Boeing Company for NASA-Lewis Research Center under Contract NAS3-13232. The program objective was to apply integrated electronic circuits technology to the design and fabrication of flexible, integrated modules of thin-film cadmium sulfide solar cells.

While interest in thin-film CdS solar cells is generally due to the low-cost potential, this advantage will be fully realized only if the cells can be incorporated into large area arrays with minimal manual assembly operations. Thus, some means must be developed for low cost, high-production-rate assemblage of large segments or modules of interconnected single cells. The purpose of this program was, therefore, to explore the possibility of applying the interconnection techniques developed for microelectronic integrated circuits to fabricate the integrated modules and thereby establish a technology framework upon which the future construction of low cost large area arrays could be based. For example, if the vacuum metallization techniques routinely used to interconnect components in integrated circuits could be applied towards interconnecting the thin-film solar cells during cell fabrication, a significant improvement should result in array cost and geometrical tolerance considerations when compared to the present techniques using conductive epoxies or solder to join individual units.

The application of integrated circuit technology was not to be limited only to cell interconnections, but included the fabrication of the single cell or basic photovoltaic device. Previous CdS single cells (refs. 1, 2, and 3) were formed by vacuum-depositing n-type CdS onto a flexible, 1-mil-thick kapton plastic substrate that had a zinc-plated conductive coating applied to one side. After masking the edges of the CdS film, (e.g., with tape), these films were immersed in a heated, aqueous solution saturated with CuCl to form the Cu<sub>2</sub>S barrier layer. A metal-mesh grid was then bonded to the barrier layer with conductive epoxy. A cover plastic was applied to provide environmental protection and to prevent cell curling that results from unbalanced thermal stress conditions. These 54 cm<sup>2</sup> cells were typically 3 to 4 percent efficient in AMO sunlight at 25°C.

The present program, which combined the past CdS thin-film solar cell studies with integrated circuit techniques, consisted of the design of a general module configuration, a submodule, and a single cell; development of single-cell technology; fabrication of single cells and submodules; characterization of critical processes and materials; testing single cells and submodules; and delivering single cells, submodules, and components.

While the total work effort was to include developing both a single cell and a submodule containing three series-connected cells, during the first year's effort all of the experimental activity was confined to the single cell. A major portion of the second year's effort was devoted to developing 3-cell submodules using a dry barrier formation process. The efficiency goal for a 30 cm<sup>2</sup> single cell was 3 percent at 25°C under AMO illumination.

Cell fabrication included the following items: metallized plastic substrates, vacuum deposited CdS films; barrier layer formation by the CuCl dip technique (early in the program) or by a dry (vacuum) process (developed later in the program); vacuum-deposited collector grids and cell interconnections; and plastic encapsulation of the cells.

## INITIAL DESIGN CONCEPTS

At the start of the program a design was prepared for the single cells and modules to serve as a guide in their experimental development. Information such as detailed geometrical drawings, general material specifications, descriptions of planned fabrication procedures, and the expected device performance was included in the design.

The design was developed by combining applicable integrated circuit technology with the known thin-film solar cell technology. Consequently, it was based upon a kapton plastic substrate, vacuum deposited CdS films, and barrier formation with hot CuCl solutions as described in the CdS solar cell literature. The IC influence was apparent in the planned design in the form of the substrate metallization (vacuum metallizing with chromium the copper-clad kapton), vacuum evaporated gold grids, and vacuum evaporated interconnections between single cells. It was also planned to use an evaporated film process for barrier formation (coevaporation of  $\text{Cu}_2\text{S}$  and CdS) so that the entire cell could be formed in a single atmosphere, i.e., vacuum.

As could be expected, these original ideas were modified and updated based on experience and new knowledge acquired during the course of the program. The modifications and other developments leading to the evolution of a new design are described, where appropriate in other sections of this report.



## VACUUM DEPOSITION FIXTURE

A deposition fixture capable of manipulating deposition masks and vapor sources by external controls was required to deposit all of the cell layers without breaking vacuum. The fixture was designed for construction onto a feed-through ring that could then be placed on the base plate of a vacuum chamber. The chamber selected for the cell fabrication was a liquid-nitrogen-trapped, oil-diffusion-pumped system with an ultimate vacuum of  $5 \times 10^{-8}$  torr.

The fixture was built with provisions for five deposition masks and 12 vapor sources. It also contained a substrate heater based upon two banks of quartz infrared lamps, two quartz crystal microbalances, and liquid-nitrogen-cooled shroud. The electrical instrumentation, thermocouple, high current, high voltage, liquid nitrogen, and mechanical motion feed-throughs necessary to operate these various fixture components were mounted on the feed-through ring. A variable leak valve, nude ionization gauge, and thermocouple vacuum gauge also used in the program were included as part of the vacuum chamber. The major fixture components just described are fairly apparent in figures 1a and 1b, which are overall views of the deposition fixture.

As mentioned previously, the substrate heater consisted of multiple quartz lamps. These lamps were positioned experimentally such as to minimize any gradients in the substrate temperature. Using thermocouples bonded to a 1-mil-thick kapton film substrate, it was found that the temperature uniformity was within  $\pm 5^\circ\text{C}$  at  $200^\circ\text{C}$ . However, because both placing a mask in front of the substrate and the deposition of a film affects the temperature, it was not known what the temperature spread was during an actual cell deposition. To minimize these effects, a thermocouple was placed on the backside of each substrate in proximity to the CdS film.

Two quartz crystal microbalances were used to control the deposition rates and thicknesses of all films in the cell structure, one for all depositions other than the CdS, and one for CdS depositions only. Because the maximum frequency shift for each crystal was about 80 kHz, it was necessary to place screens in front of the crystals--about 10 percent transmission on the CdS crystal holder and 50 percent on the other film monitor.

Very early in the program, all substrates were glow-cleaned in argon at a chamber pressure of 30 to 50 microns. The cleaning fixture consisted of a shielded ring, with the inner conductor being held at a high negative potential with respect to the grounded shield and vacuum chamber. As the program progressed, however, there appeared to be little benefit from the cleaning; e.g., no effect on film adherence or pin holes was detectable. In fact, because of the unwanted deposition of residual CdS onto the ring, which could then be sputtered onto the substrate during the cleaning operation, glow cleaning was discontinued and the ring removed from the fixture.

For the film depositions, the plastic substrates were clamped in the two-piece, removable holder shown in figures 2a and 2b. The outer substrate holder or frame was suspended from the top fixture plate by four stringers. Bolted onto the frame was the inner holder (see figure 2b) that contained the plastic

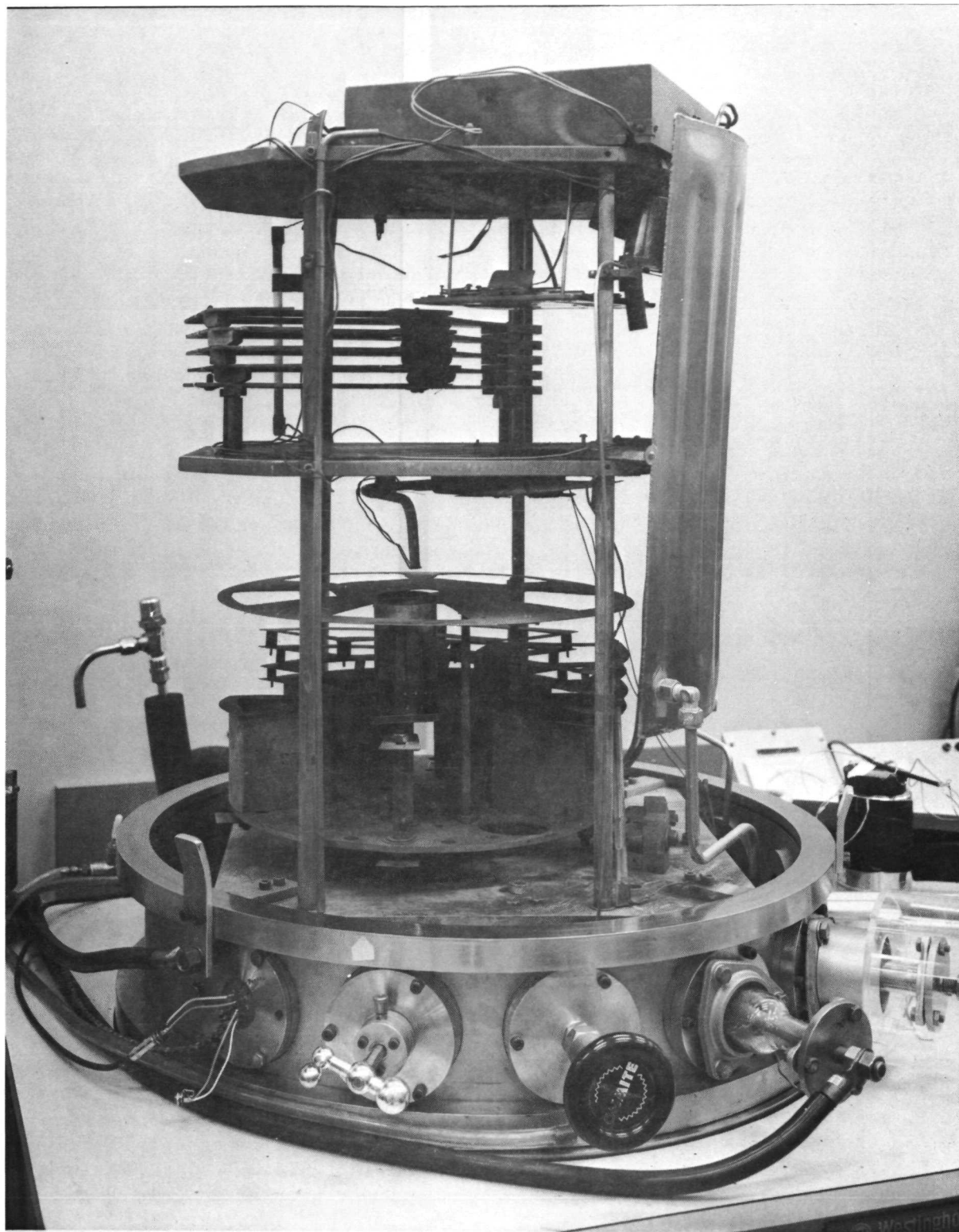


Figure 1(a): OVERALL VIEW OF DEPOSITION FIXTURE (SIDE)

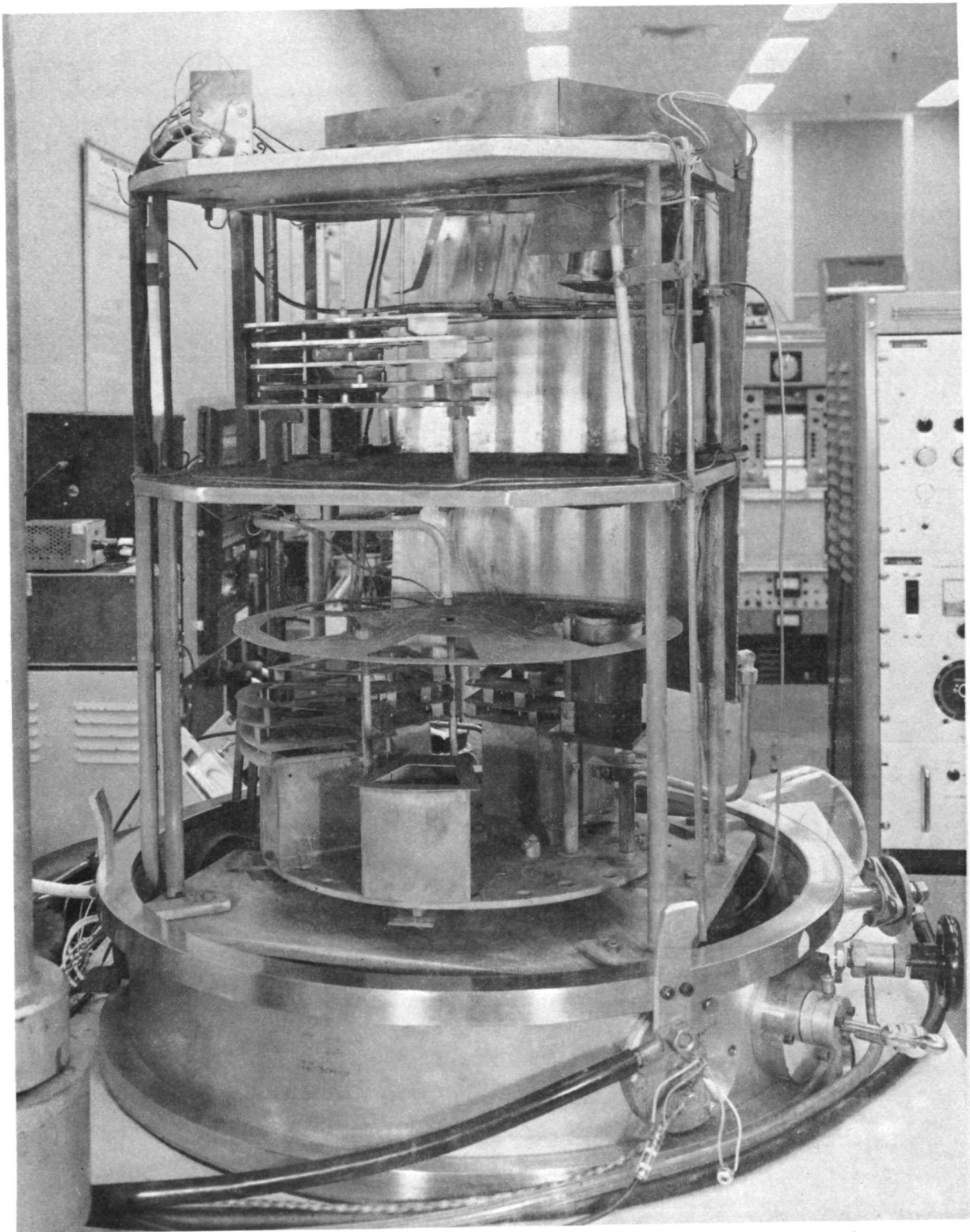


Figure 1(b): OVERALL VIEW OF DEPOSITION FIXTURE (FRONT)

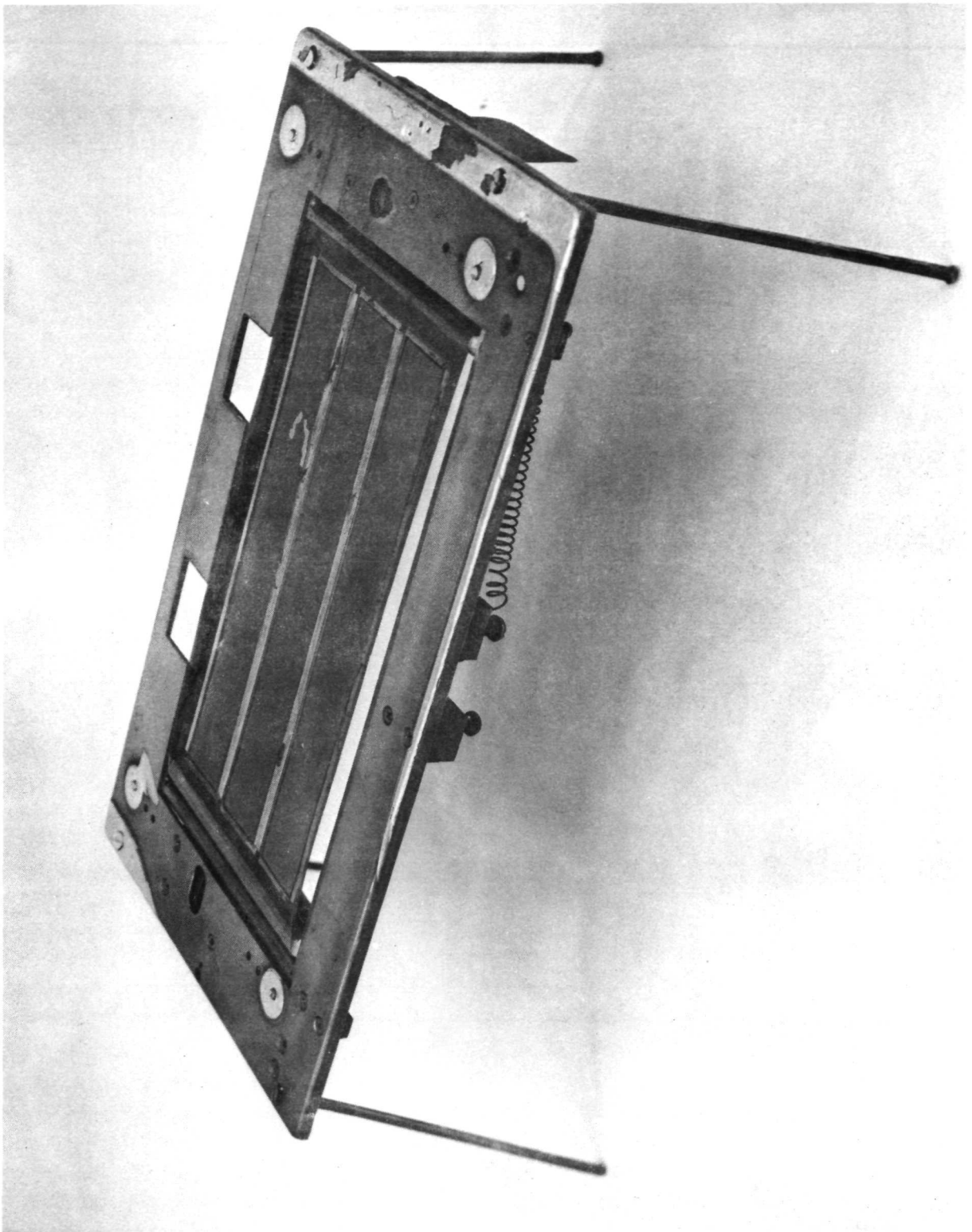


Figure 2(a): ASSEMBLED, COMPLETE SUBSTRATE HOLDER WITH DEPOSITED SUBSTRATE



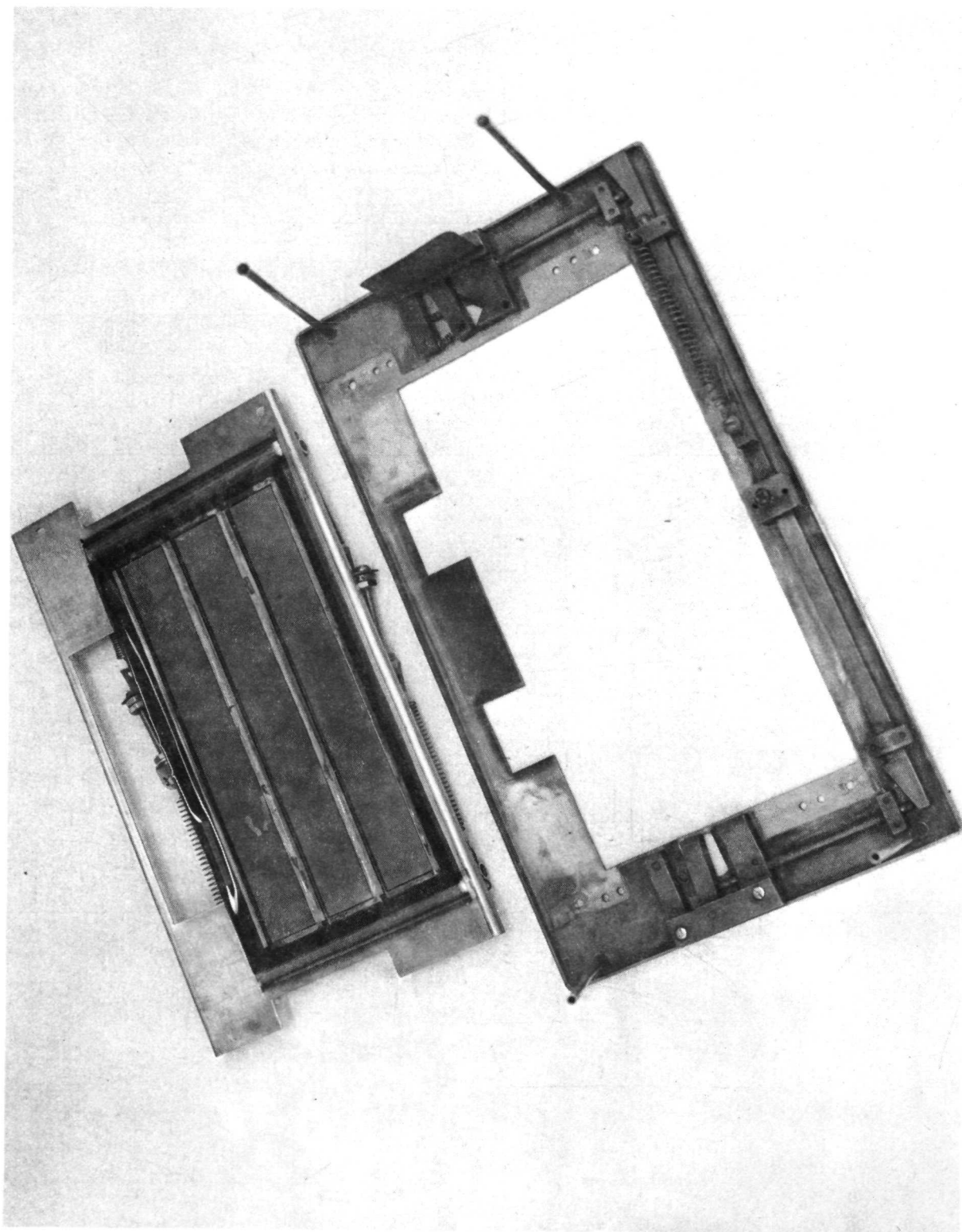


Figure 2(b): INNER AND OUTER COMPONENTS OF SUBSTRATE HOLDER

substrate. The inner holder was spring-loaded to flatten the plastic against a glass plate. It should be noted that the substrates were normally not removed from the inner holder (stainless steel) when the substrates were in the cleaning barrier formation or etching solutions. Leaving the substrates in the holder greatly simplified the handling and subsequent mask alignment problems.

The deposition masks were aligned to the substrate and to each other by a system of V blocks and pins. The V blocks were mounted on the frame part of the substrate holder (fig. 2) and were operated by a flexible wire cable attached to a motor. The pins were press-fit into the individual mask holders. All of the deposition masks were fabricated with alignment holes to match the pin locations. The actual alignment operation of the fixture is depicted in figures 3a and 3b. Thus, after the desired mask/mask holder was selected, it was swung (fig. 3a) under the substrate holder and then raised. As the mask holder was lifted, the registration pins slid through the open V blocks until the mask holder actually carried the substrate holder (fig. 3b). At this point, there should be good contact between the masks and the substrates. The V blocks were then closed for the film deposition followed by reversal of the procedure outlined above.

A second chamber was required later for the  $\text{CuCl}$  deposition used in the fabrication of cells by a dry barrier formation process. This system, figure 4, was similar to that described above, except it has no provision for multiple masks and vapor sources. This chamber contained the same instrumentation and substrate heater, but did not have the mechanical versatility of the other system.

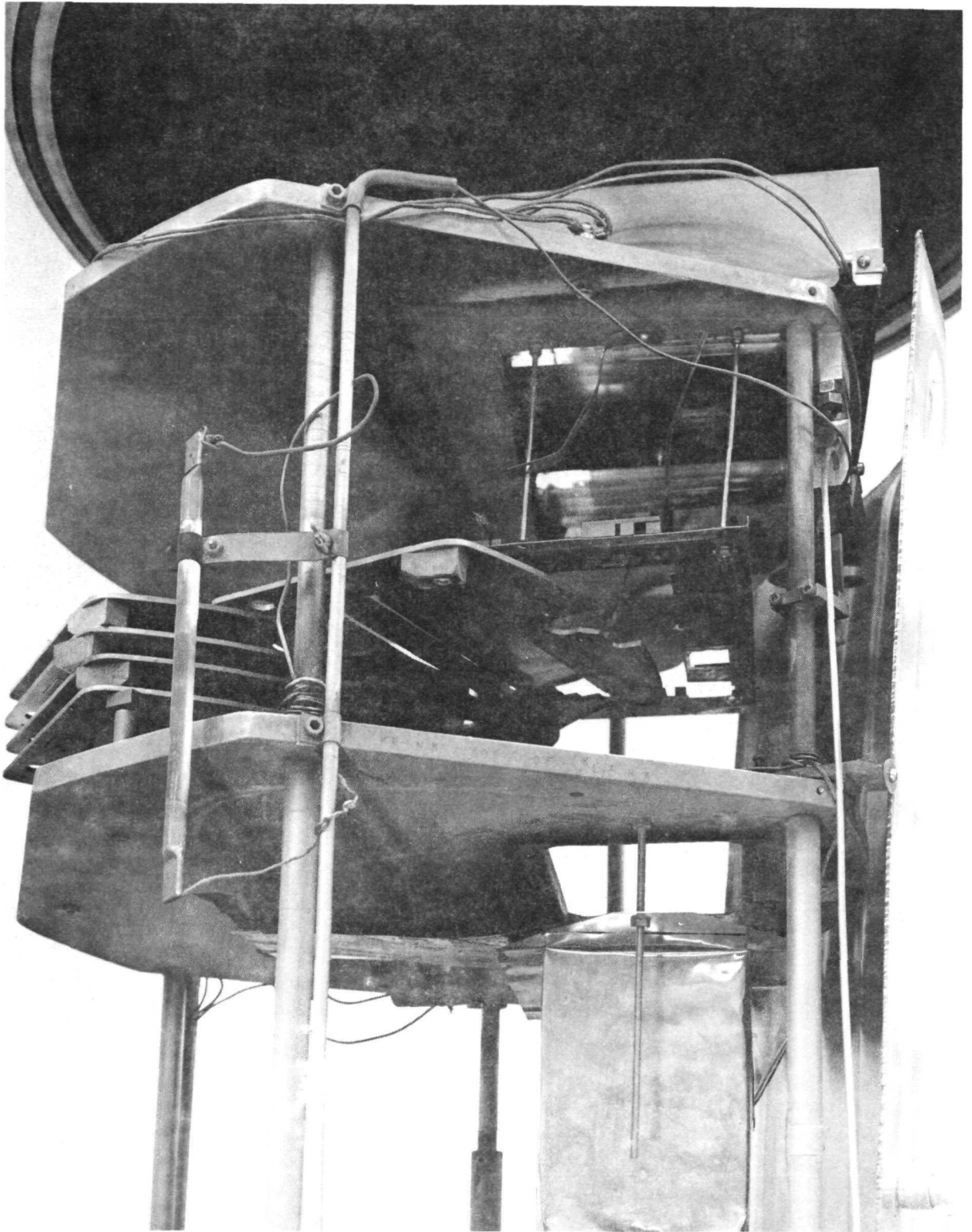


Figure 3(a): DEPOSITION FIXTURE DURING MASK SELECTION/REGISTRATION SEQUENCE

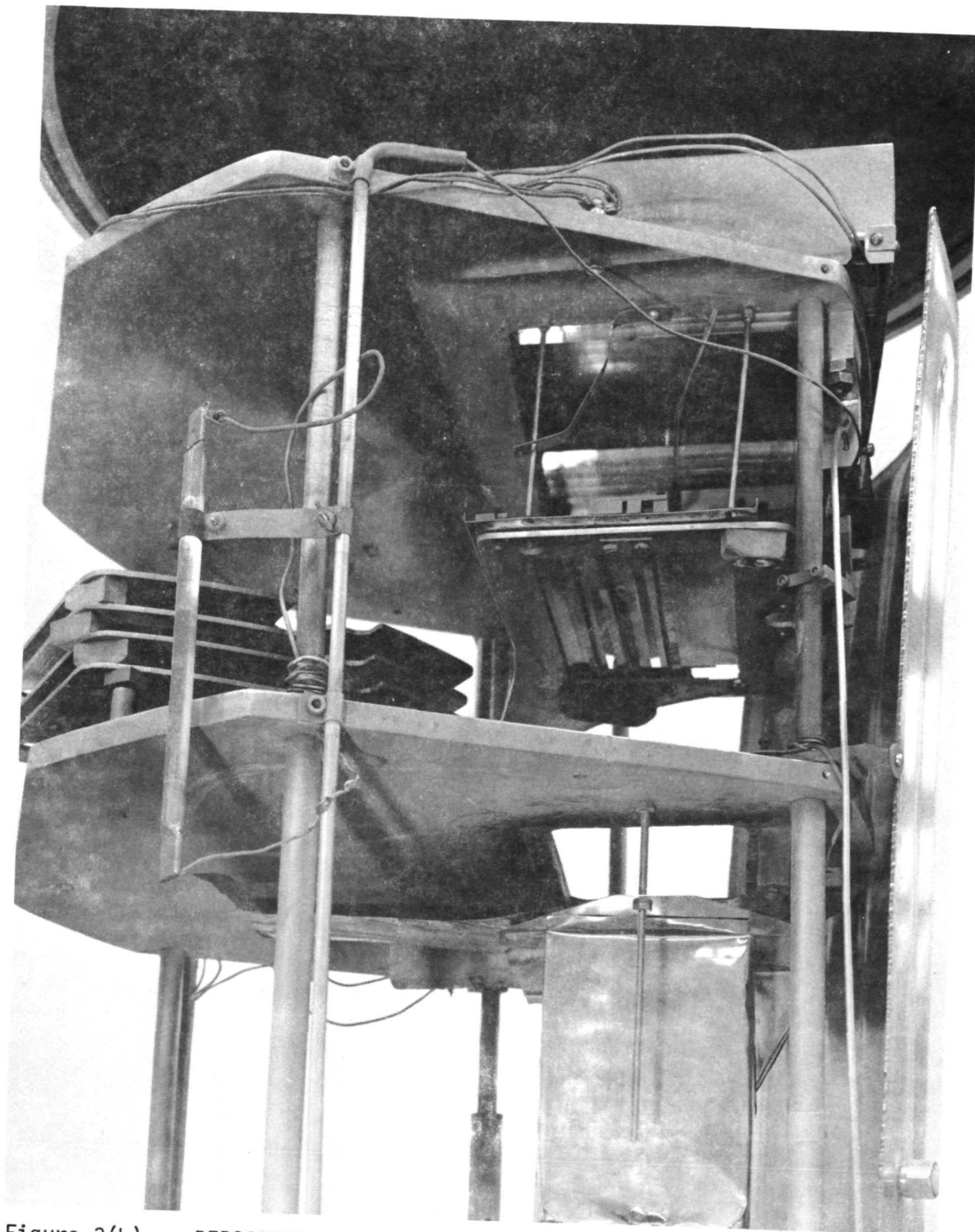


Figure 3(b): DEPOSITION FIXTURE WITH MASK REGISTERED TO SUBSTRATE HOLDER



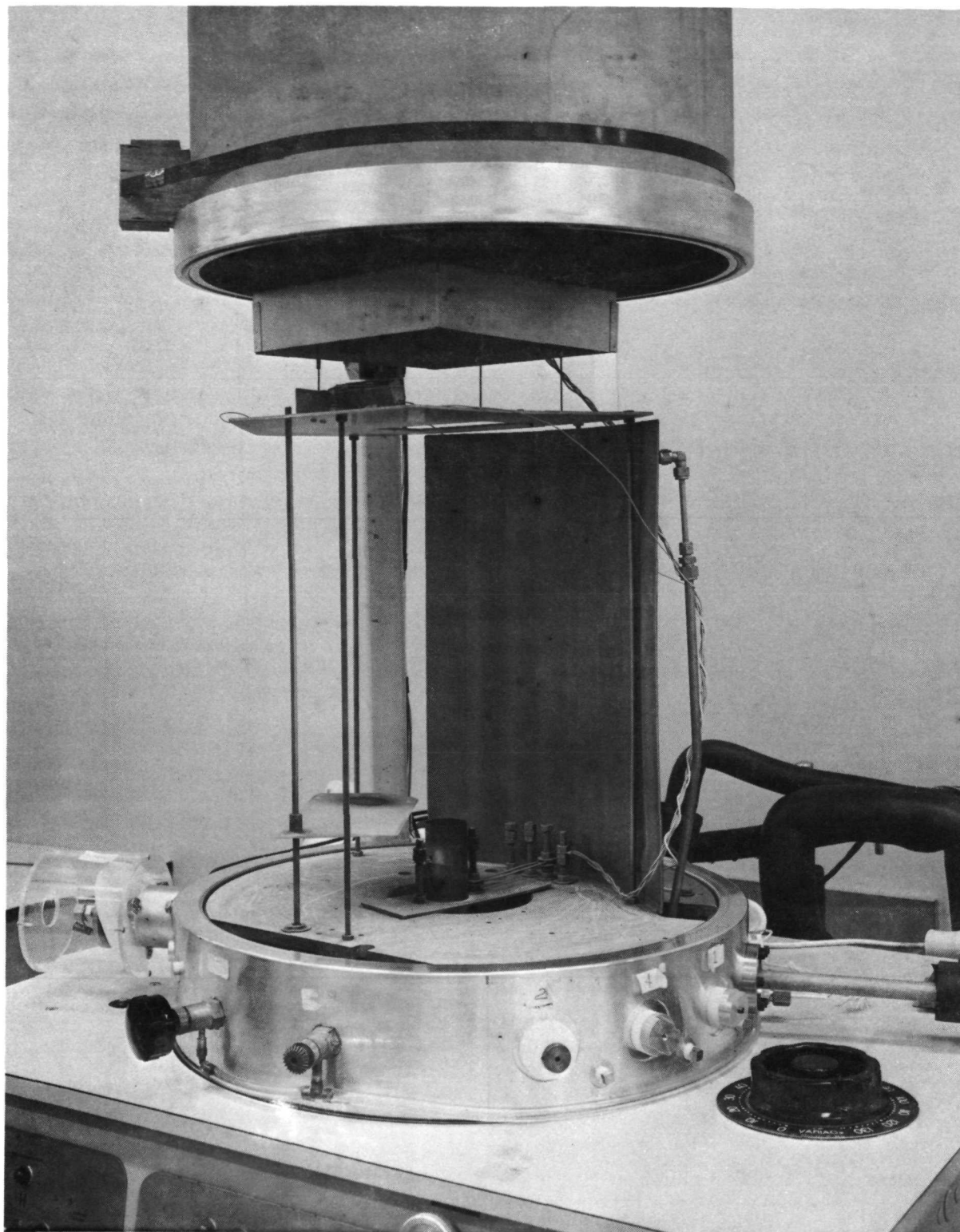


Figure 4: OVERALL VIEW OF  $\text{CuCl}$  DEPOSITION FIXTURE

## CELL TEST FIXTURES

### I-V Characteristics

The fixture constructed for testing the CdS cells and modules consisted of four independently controlled Sun-Gun lamps, a 2-inch-thick light filter containing a 1-gm/L copper sulfate solution, a temperature-controlled vacuum holddown chuck, and a Spectro-Lab Model D-550 electronic load with X-Y recorder. The system is shown in figure 5.

The chuck temperature was controlled by varying the temperature of water flowing through passages in the chuck. An adjustable range controller-recorder driven by a thermocouple sensor imbedded in the chuck closed the loop on the temperature control system. The system was capable of controlling the chuck temperature to  $\pm 0.5^{\circ}\text{C}$  at the required  $25^{\circ}\text{C}$  and  $60^{\circ}\text{C}$  cell-testing temperatures.

An airplane-flown calibrated CdS standard cell provided by NASA/LeRC was available in the laboratory for final adjustment of the lights to AMO conditions. A silicon cell was used as a secondary standard for preliminary measurements early in the program, but was soon replaced with the CdS standard cell for a better calibration.

Practically all test results on the fabricated CdS cells were conducted under these approximate one-sun conditions at room temperature using gold-tipped probes to contact the barrier layer and the gold-covered negative electrode.

### Spectral Response

The spectral response apparatus, which was developed late in the program, is shown schematically in figure 6. A high-intensity quartz-iodine lamp was used as the light source, focused by external mirrors onto the monochromator entrance slit. The monochromator was a Perkin-Elmer Model 99 single beam, double pass instrument. White bias light, adjusted to an intensity of  $25\text{mw}/\text{cm}^2$ , was supposed to be provided by a quartz-iodine lamp mounted on a bracket just outside the exit slit of the monochromator. Unfortunately, the bias lamp was damaged and a replacement was late in arriving so that measurements under bias light conditions were never obtained.

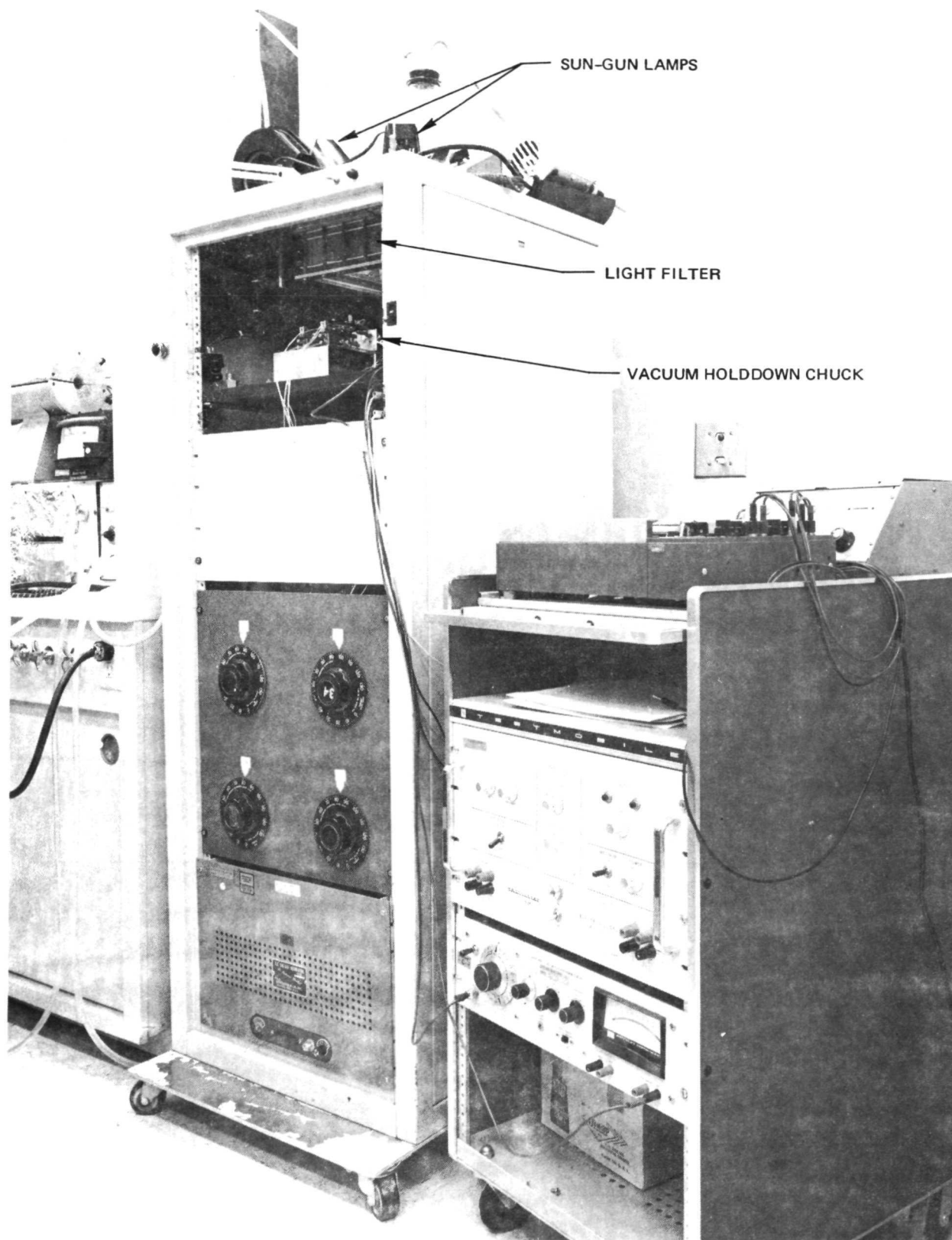


Figure 5: V-I CELL TESTING APPARATUS

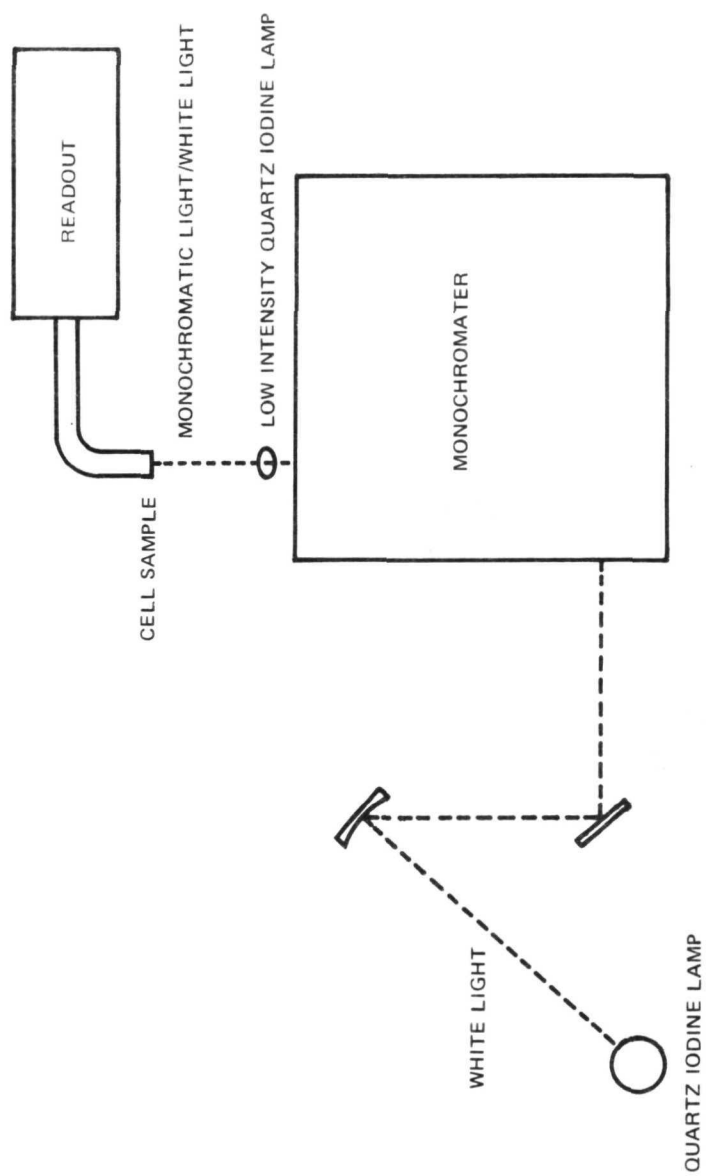


Figure 6. SCHEMATIC OF SPECTRAL RESPONSE APPARATUS

## DEPOSITION MASK FABRICATION

The metal, stencil-type masks used in this program were fabricated using techniques common to the thin-film hybrid integrated circuit field. That is, the first step was to make an engineering drawing for each of mask configurations corresponding to the separate, deposited cell layers. The enlarged drawings were made at 25.4 X to simplify the English to metric conversion. A coordinator graph was used to transform the drawings into highly accurate layouts by cutting the ruby studnite film. After peeling the red layer from the cut studnite in the areas that were to be transparent during photo processing, the layouts were photo-reduced. With the width of the cell being 15 cm, it was decided to complete only a small portion of each layout and then step (six times) this pattern on the photo-reduction camera. Thus, on the grid mask, instead of drawing some 300 grid lines only 50 were necessary.

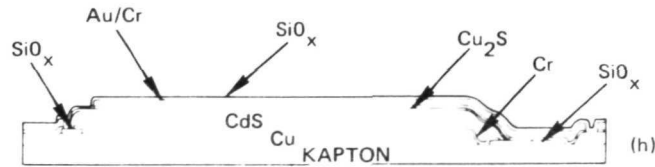
Glass master negatives of the final size for each of the masks were produced by the camera. The CdS mask-master also contained the patterns for a Hall sample and for an optical absorption sample. All of the masters contained the alignment holes and slots to mate with the pins on the mask holders. The masters were used to expose photoresist-coated 5-mil beryllium-copper mask stock material. After developing the resist, the masks were etched to form the required patterns.

Because of the fine detail in the grid mask, i.e., 2-mil lines on 20-mil centers, the standard one-sided etching techniques were not acceptable. Instead, grid masks with 2-mil lines were fabricated by a gold-kovar method where a -0.25-mil plated gold layer supported by an over-etched kovar mask defined the detailed mask pattern.

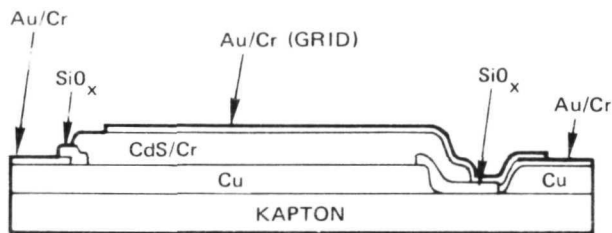
As experimental data was acquired, it became apparent that modified masks should be made. Modifications to one mask usually required a change in others, so mask sets were formed. Six of the sets were formed (labeled A through F). The differences between these masks are shown in figure 7, which contains sketches of cell cross sections formed with the masks. The main reason for the development of each set will be discussed below.

Mask set A. - In the original set of masks (A), the grid and contact-area films were deposited through the same mask. With this geometry, the masks became distorted upon etching and had poor tolerances because of the widely different etching rates for the fine grid lines in contrast to the contact areas. Furthermore, copper in the contact areas would be exposed to the various environments encountered during barrier formation (including a 250°C air bake) because the protecting gold films would not be present until the grids were deposited.

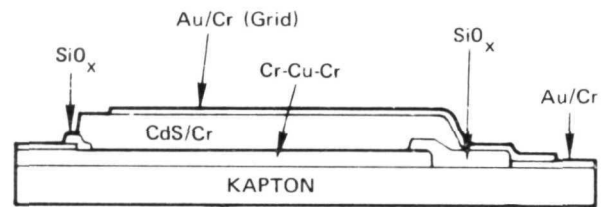
Mask set B. - Because of the problems noted above with the A masks, a new series of deposition masks was designed. Thus, mask set B mainly separated the grid from the contact areas and was the basic set used for the copper-clad kapton substrates.



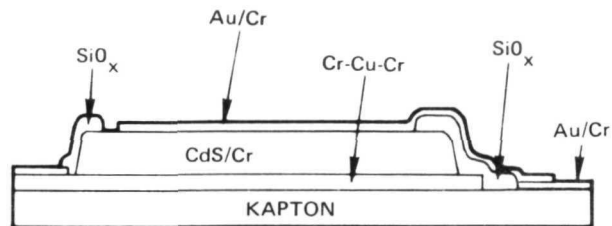
(a) MASK SET A—CELL CONSTRUCTION ON COPPER-CLAD KAPTON



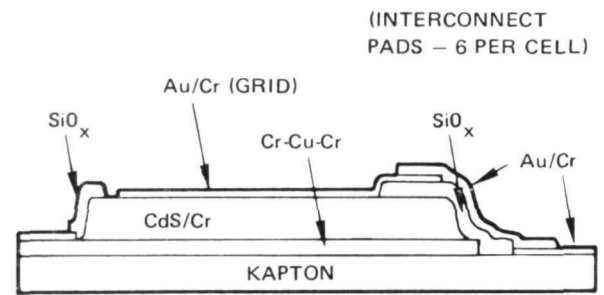
(b) MASK SET B—COPPER-CLAD KAPTON SUBSTRATE



(c) MASK SET C—PLAIN KAPTON SUBSTRATE



(d) MASK SET D—PLAIN KAPTON SUBSTRATE



(e) MASK SET E—PLAIN KAPTON SUBSTRATE

Figure 7. SKETCHES OF CELL CROSS SECTIONS FORMED WITH MASK SETS A THROUGH E

Mask set C. - As the program progressed, the advantages of using a vacuum-metallized kapton substrate became apparent. Mask set C was designed and fabricated for depositing the cell layers onto a plain kapton film. The cell geometries were essentially identical to those of sets A and B.

Mask set D. - Mask set D was a slight revision to set C, which allowed the metallization mask to be extended. The entire CdS layer could be deposited over the metal film to achieve high adherence at the CdS film edges.

Mask set E. - In set E, the combined grid and cell interconnect functions common to all previous mask sets were separated into two masks. The reason for this separation was to reduce from 300 to 6 the number of points where the metal film crossed over the edge of the thick CdS deposit. Thus, the requirement for highly adherent CdS along the entire length of the film edge could be substantially relaxed. Other than this change, the remaining masks in the set E were approximately the same as set D.

Mask set F. - Mask set F was the same as the single cell masks of set E with the additional feature of providing interconnection for 3-cells in series, i.e., this was the submodule mask set. The plan and cross-section views of the module and individual cells resulting from use of this mask set are depicted in figure 8. The intercell spacing shown in figure 8 is much larger than necessary to facilitate the dicing of the submodules into single cells for separate processing studies. Some of the critical dimensional characteristics of units formed according to mask set F are listed in table I.

TABLE I: DIMENSIONAL CHARACTERISTICS OF SUBMODULE AND SINGLE CELLS

DIMENSIONAL CHARACTERISTICS OF SUBMODULE AND SINGLE CELLS	
SUBMODULE	
TOTAL SUBSTRATE AREA	- 114.3 cm <sup>2</sup>
CELL ACTIVE AREA	- 90.0 cm <sup>2</sup>
AREA UTILIZATION (INCLUDING INACTIVE TEST AREAS)	- 0.79
AREA UTILIZATION (EXCLUDING INACTIVE TEST AREAS)	- 0.92
GRID WIDTH	0.05 mm
GRID SPACING	0.5 mm
INTERCELL SPACING	0.6 mm
SINGLE CELLS	
SUBSTRATE AREA	- 32.4 cm <sup>2</sup>
CELL ACTIVE AREA	- 30.0 cm <sup>2</sup>
AREA UTILIZATION	- 0.93
GRID WIDTH	- 0.05 mm
GRID SPACING	- 0.5 mm



Figure 8. *CdS SOLAR CELL SUBMODULE*



## CELL FABRICATION---WET PROCESS

As indicated previously, CdS thin-film cells of the front-wall type were fabricated on metallized kapton substrates using through-mask vacuum-deposition techniques. The cell structures were deposited onto both copper-clad kapton and vacuum-metallized kapton substrates. In both cases, a  $\text{Cu}_2\text{S}$  barrier layer was formed on the CdS surface by immersing the samples into a heated, aqueous solution of  $\text{CuCl}$ .

### Substrate Materials and Preparation

A commercially available copper-clad kapton was studied as a possible substrate for the cells because of its high sheet conductivity and expected reproducibility in surface characteristics. The copper-cladding was approximately 0.7-mil thick on the 0.9-mil-thick kapton. While the copper thickness was greater than that required to achieve a sheet conductivity of higher than 0.01 ohm per square, this was the minimum value recommended by the manufacturer for layers having a reasonably low pinhole density.

The procedure described below was evolved for preparing the clad substrates. After cutting the bulk material to the required substrate size, the substrate was taped to a rigid backplate to facilitate cleaning, photoresist application, and etching. The photoresist etching process was necessary to form the metallization gap between electrodes on the cell. The resist was applied by the spin technique after rinsing the mounted substrate with trichloroethylene. This operation was followed by baking, exposing, etching, and finally resist removal. To round the metallization at the gap edges (fig. 9), the substrate was then rolled around a mandrel so that the copper surface formed the outer circumference of a 3-inch-diameter cylinder. A 2-inch-diameter piece of stainless steel tubing formed the counterelectrode. Both electrodes were immersed in an electroplating bath of the following composition:

<u>Material</u>	<u>Composition (parts by weight)</u>
$\text{H}_2\text{O}$	100
$\text{CrO}_3$	12.5
$\text{Na}_2\text{Cr}_2\text{O}_7$	37.5
HAc	12.5
$\text{H}_2\text{SO}_4$	10.0

The copper substrate was made anodic and electropolished for 5 minutes at 90 ma/in<sup>2</sup>. After polishing, the substrate was rinsed and hand-burnished with 600-grit silicon carbide. The burnishing flattened small imperfections in the copper layer (e.g., those shown in fig. 10) which had been further intensified by the electropolishing. The substrates were then rinsed with DI water, dried, and stored in a desiccator.

As a substrate for a CdS cell, the copper-clad kapton exhibited a number of undesirable features that became apparent with the fabrication of cell structures. For example, the copper layer was found to contain imperfections of the

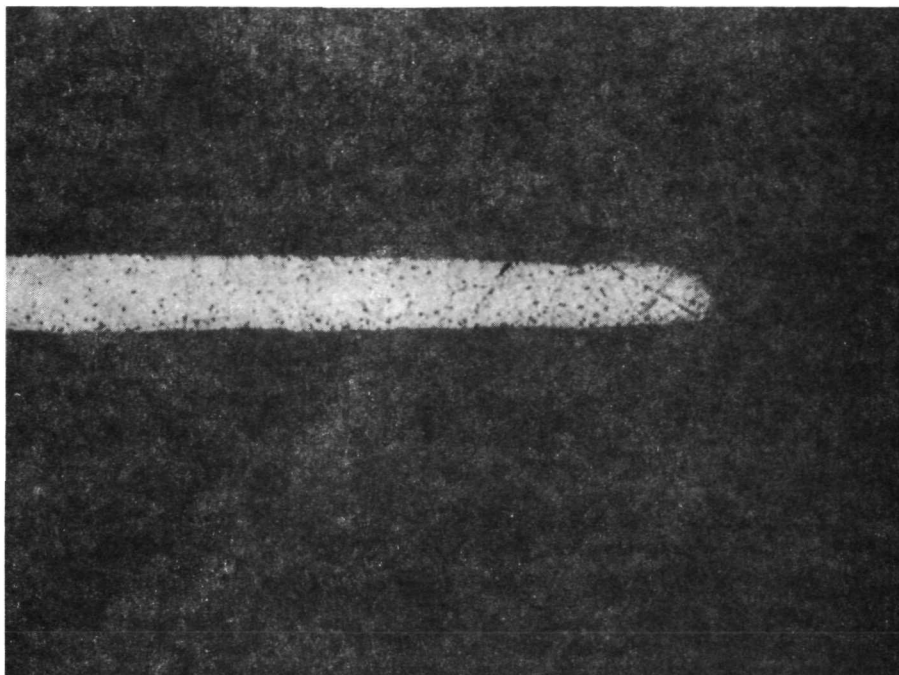


Figure 9: EDGE OF ETCHED COPPER CLADDING ROUNDED DURING SUBSTRATE PREPARATION (1000 X)

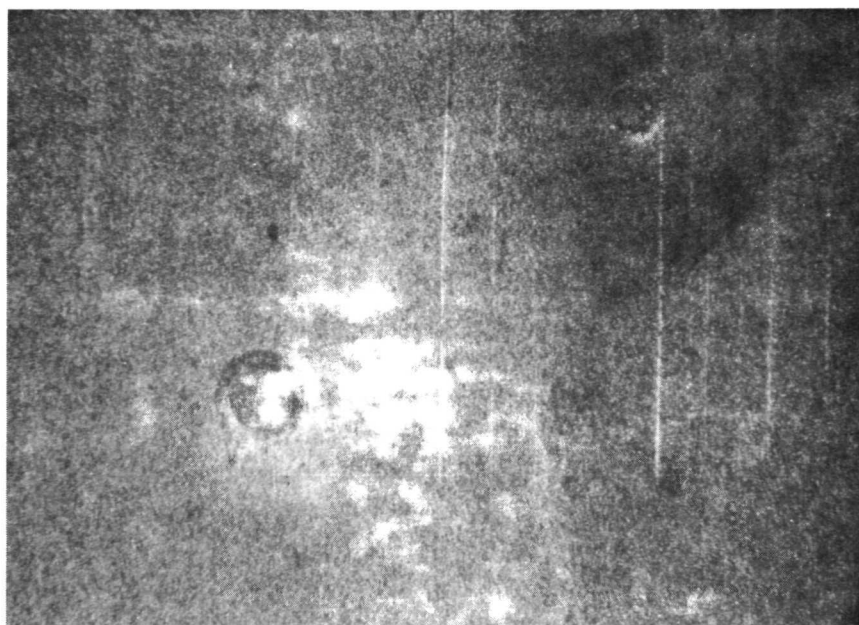


Figure 10: PINHOLE-TYPE IMPERFECTION IN COPPER CLADDING (25 X)

type shown in figure 10. These defects appeared as pinholes with mounds around the rim. However, because copper was present on the bottom of the defect, they were not pinholes in the usual sense. As the CdS would replicate these structures, they were considered to be undesirable, and the substrate preparation process was adapted to minimize their effect on the surface smoothness.

Other problems encountered with the copper-clad substrates were delamination following the film depositions, assuring round corners and tapered edges in the metallization gap region, and alignment of the etched substrate in the vacuum-deposition fixture. Because of these disadvantages, techniques were developed to utilize plain 1-mil kapton film as a substrate that was vacuum-metallized in the same deposition cycle as the other cell layers.

The kapton was cleaned before metallization by rinsing in DI water, ultrasonic cleaning in a hot DI water-detergent solution, cold DI water rinse, and finally blown dry with high-purity nitrogen.

### Single-Cell Deposition Processes

Chamber instrumentation. - The vacuum chamber that contained the deposition fixture for cell fabrication was instrumented such that the following parameters were monitored or controlled: (1) CdS source temperature and power input (voltage and current were monitored); (2) total chamber pressure; (3) film thickness; (4) film deposition rate; and (5) substrate temperature. All of these parameters were plotted on a multichannel strip-chart recorder so that a permanent record of the deposition parameters for each cell was retained.

CdS vapor source. - The CdS source developed for this program was a double-walled fused-quartz crucible. The inner tube was about 0.5 inch in diameter and the outer 1.25 inch in diameter. The crucible was usually 3 inches in height and was packed on top with quartz wool to prevent spattering of the CdS particles. For the source-temperature measurements, a small quartz tube containing a chromel-alumel thermocouple was inserted through the quartz wool cap into the CdS powder. Typically, the temperature was 1100° to 1200°C.

The source was heated by inserting a tungsten helix into the entire length of the inner tube. The crucible source was then placed within thin tantalum sheet radiation shields. Because of the radiation shields and location of the heating element inside the CdS powder, the chamber outgassing was reduced such that pressures near  $1 \times 10^{-5}$  torr were maintained during the CdS deposition.

Preparation of CdS powder. - Prior to deposition, the CdS powder (General Electric, Electronic Grade, Type 118-8-2) was prepared by vacuum bake and sintering operations similar to those reported by other investigators. For example, the procedure reported in ref. 1 utilizes a 900°C vacuum bake followed by an argon bake at 1200°C. In the present program, this operation initially consisted of placing 1 pound of the powder-between quartz wool packing in a quartz tube contained in a high-temperature tube furnace. The tube was evacuated with a liquid-nitrogen-trapped mechanical pump to 15 to 25 microns. For safety precautions, the pump was exhausted into a fume hood. The furnace was heated to 700°C and held for 6 hours, then allowed to cool overnight while still under vacuum.

Following the vacuum bake, the tube containing the CdS was back-filled to atmospheric pressure with high-purity (99.996 percent) argon. The argon flow rate was adjusted to 400 cc/min., with the tube outlet again exhausting into a fume hood. The tube was heated to 1100°C and held there for 4 hours. After cooling the furnace while maintaining the same argon flow rate, the CdS powder now partially sintered and much more dense, was removed.

For the first several batches of processed CdS, the baked material was ground in a porcelain mortar and pestle to pass a 48 mesh Tyler screen. This procedure was then modified to only breaking up the sintered powder with a quartz rod and eliminating both the grinding and screening. The reasons for making this change were concern of aluminum contamination from the porcelain and pin-hole generation in the CdS film resulting from the "fines" produced by grinding.

On the advice of the Lewis Contract Monitor this bake operation was altered to essentially that used at the Lewis Research Center. This was baking in an argon flow of 400 cc/min. for 64 hours at 800°C followed by a 8-hour bake at 1200°C again in argon. The effect of the bake conditions on the properties of CdS films is discussed further in the Analytical Studies section (Scanning Electron Microscope).

Substrate metallization. - After etching the copper-clad kapton substrates to develop the cell metallization gap, it was necessary to coat the copper with a material that formed an ohmic contact and displayed high adherence to the CdS film. A chromium thin-film (500 Å) vacuum-deposited from a tungsten boat immediately before the CdS was found to give excellent results; i.e., the I-V characteristics of the contact indicated ohmicity and the thick CdS films (~1-mil) adhered very strongly.

When the plain kapton film was used as a substrate, it was coated with several different vacuum-metallized materials. Initially, only chromium was used. However, the sheet resistivity of chromium films was excessive because of the high bulk resistivity and poor chamber environment during the film deposition. To achieve metallization resistivities of less than 0.1 ohm per square would have required chromium film thicknesses that were impractical by normal vacuum-deposited techniques.

Aluminum films of 0.5 to 1.0 micron were then deposited from a boron nitride crucible source onto kapton substrates heated to 200°C. Sheet resistivities from four-point-probe measurements were in the 0.06 to 0.08-ohm-per-square range. Using the film thickness values, it was determined that the lowest film resistivity was 3.4 ohm-cm versus 2.65 for bulk aluminum.

Although the aluminum films displayed the desirable high sheet conductivities, they did not adhere as strongly as chromium to the kapton substrates or to the CdS films. Consequently, a chromium film was used as an interface between the aluminum and CdS films.

Cell structures based on the aluminum metallization were discovered to be unsatisfactory during the barrier formation studies where the substrates were immersed in the CuCl solution. Plating of metallic copper during this treatment occurred readily and extensively over the CdS covered cell area.

Because of the plating problem, the substrate metallization was changed to vacuum-deposited copper films. The copper films were deposited from an alumina crucible, and for the thickness of about 1 micron the sheet resistivity was determined to be 0.05 ohm per square. To achieve adherence to the kapton and ohmic contact/adherence to the CdS, the copper film was sandwiched between two thin chromium films. The first chromium film was then replaced by nichrome to reduce the occurrence of delamination between the substrate and the copper films.

Film depositions. - To control and monitor the film-deposition rates and thicknesses used to form the single-cell structures, calibration constants were determined for each material that related the frequency shift on the quartz crystal microbalance to the true film thickness. The film thickness was obtained using a multiple beam interferometer or talysurf. The calibration was straightforward except for the CdS. Depositing a film with a thickness in the 1-mil range required placing a screen-aperture (about 10 percent transmission) in front of the crystal. In addition, the crystal was water-cooled in contrast to the 200°C substrate. The combination of these effects resulted in a monitoring accuracy of only  $\pm 20$  percent for the CdS. The film-thickness data were periodically confirmed by analyzing cross sections of the films.

The typical conditions under which the films contained in the single-cell structure were deposited are shown in figure 11. This figure is a copy of a standard laboratory fabrication form used to control the fabrication of a thin-film circuit or device and also serves as a convenient summary record of the deposition parameters actually used in the unit fabrication.

Following completion of the deposition cycle, cooling of the substrate to near room temperature, and back-filling the chamber to atmospheric pressure with high-purity nitrogen, the substrate was removed and stored in a nitrogen-purged dry box.

#### CdS Film Spray

One of the most difficult tasks encountered during the early phase of the wet process program was the control of CdS spray beyond the film edge defined by the deposition mask. This spray or surface migration of the CdS differed from the usual thin-film spray in that it extended in some cases to as much as 0.5 inch from the film edge. Although this spray occurred on all four sides of the CdS film, it was much more severe on the edge adjacent to the metallization gap of the cell structure. Because of its presence in this region and the fact that (especially when the substrates were immersed in the barrier formation solutions) the spray was nonadherent or resulted in a nonadherent base for subsequent films leading to shorted cells or preventing cell interconnection, considerable effort was expended to bring the spray under control.

One approach mentioned previously was to extend the metallization such that all of the CdS was over chromium. With the known high adherence of CdS to chromium, it was believed that the spray could be made more adherent. While the extension did yield some benefits, it became apparent that further improvements were necessary. These were achieved by: (1) installing a glass plate in back of the kapton substrate to improve the kapton flatness during CdS deposition; (2) modifying the substrate-mask-holder alignment procedure and mask-support system to improve the

PROJECT CdS CELLS	ENGR ASSIGN MICKELSEN	TECH ASSIGN WOLFF	SYS ASSIGN 10	APPROVED BY	CIRCUIT NO 05E6 23 /0	DATE	HOURS
JOB DESCRIPTION							
SPECIAL INSTRUCTION							
WEIGHT CdS 80 64 GMS							
WEIGHT QTZ WOOL 1 10 GMS							
DEPOSIT NO.	1	2	3	4	5	6	7
MASK NO.	NONE REV SIDE	E1	E1	E1	E2	E3	E4
SOURCE MATERIAL	SiO	Cr	Cu	Cr	CdS	SiO	Cr
SOURCE TYPE	W BASKET	W BOAT	Al <sub>2</sub> O <sub>3</sub>	W BOAT	QTZ	Ta BOX	W BOAT
SUB PREHEAT TEMPERATURE (°C)	200	200					
SUB TEMP (°C)	200	200					
REQ PRESS (TORR)	1 X 10 <sup>-4</sup>	< 1 X 10 <sup>-5</sup>	< 1 X 10 <sup>-5</sup>	< 1 X 10 <sup>-5</sup>	< 1 X 10 <sup>-5</sup>	< 1 X 10 <sup>-5</sup>	< 1 X 10 <sup>-5</sup>
ACT PRESS (TORR)	5 X 10 <sup>-5</sup>	3 X 10 <sup>-5</sup>	1 X 10 <sup>-5</sup>	2 X 10 <sup>-5</sup>	2 X 10 <sup>-5</sup>	4 X 10 <sup>-5</sup>	3 X 10 <sup>-5</sup>
REQ RATE (A/SEC)	80	10	20	10	160	60	10
ACT RATE (A/SEC)	79	10	21	11	230		9
REQ THICKNESS (A)	76,000	500	20,000	500	370,000	5,000	500
ACT THICKNESS (A)	76,000	500	20,000	500	370,000		500
REQ RES: MON (K-OHMS)							
ACT RES: MON (K-OHMS)							
REMARKS							
*CRYSTAL WAS SHIFTING, RATE THICKNESS QUESTIONABLE							
ENGR ACPT							

Figure 11. FABRICATION RECORD WITH TYPICAL FILM DEPOSITION PARAMETERS



mask-substrate contact; (3) depositing a 5- to 10-micron  $\text{SiO}_x$  film onto the back surface of the kapton substrate to greatly increase the substrate rigidity (with the  $\text{SiO}_x$  coating the substrates were nearly flat after the CdS deposition in contrast to the usual extreme curling because of large differences in thermal expansion coefficients); and (4) redesigning the grid-interconnect masks to reduce the number of points where a metal film crossed the edges of the CdS film along the metallization gap.

Other concepts, such as sputter-etching of the CdS spray, substrate temperature gradients at the CdS film edge during deposition, and applying electrostatic techniques for improved mask-substrate contact, were also considered during the experiments designed to prevent or remove the spray. These were found to be either ineffective or cause other undesirable effects. For example, the application of the high dc voltage for the electrostatic approach caused the appearance of small bumps in the metallized kapton substrate that were then replicated by the CdS film.

The procedures described for controlling the CdS spray were applicable to both the copper-clad and vacuum-metallized kapton substrates. It should be noted that the only obvious difference between structures formed on these two different substrates was the visual smoothness of the films deposited on the plain kapton. Whether a rougher film texture was advantageous to the cell operation was not ascertained but, for reasons discussed earlier, the single-cell activity progressed almost exclusively towards use of the plain kapton substrate.

#### Barrier Formation

The formation of a barrier layer on the deposited CdS films was by means of the  $\text{CuCl}$  chemical exchange process, (i.e., by immersing the films in a heated, saturated solution of  $\text{CuCl}$  in water). For this purpose, a small apparatus was constructed that consisted of a 4-liter glass beaker, a magnetic-stirrer temperature-controlled hot plate, and a nitrogen shroud with an immersed gas-dispersion tube. The shroud sealed the beaker top and purged the air over the beaker with nitrogen. Throughout the operation, nitrogen was dispersed into the solution while it was being stirred.

The usual procedure for forming the barriers was to etch the sample for 5 seconds in a 3:1  $\text{HCl}$ -to-water solution, rinse in DI water, immerse for 5 seconds in the  $\text{CuCl}$  bath heated to  $90^\circ\text{C}$ , rinse thoroughly in DI water, dry with nitrogen, and airbake for 2 to 5 minutes in a  $250^\circ\text{C}$  oven.

When the  $\text{HCl}$  etch was used prior to immersing in the  $\text{CuCl}$ , the CdS layer appeared to possess a weak, velvet-type structure. Without the etch, a smooth, blue-gray surface resulted. Although necessary to achieve high-efficiency cells, the etching greatly increased the incidence of shorted cells. In order to fabricate nonshorted cells, it was found essential to: (1) deposit the CdS in excess of 25 microns in thickness; and (2) rinse the CdS in DI water following etching.

The  $\text{SiO}_x$  isolation films deposited onto the edges of the CdS film were very effective in masking the CdS from the etchant and CuCl treatment. For example, no change in the appearance of the CdS covered by the thin (3 to 5000 Å), transparent  $\text{SiO}_x$  film were detected.

The composition of the CuCl bath itself changed very little during the study. Initially, a saturated solution (approximately 40 gm/L CuCl) modified to a pH of 3 with HCl was used. This was later altered to include the addition of NaCl to increase the solubility of the CuCl. The composition that yielded the highest open circuit voltages and short circuit currents was 16 gm/L CuCl, 16 gm/L NaCl, and 10 ml/L of 12 N HCl.

The CuCl baths were prepared by heating DI water to 90°C and then adding the HCl and NaCl and finally the purified CuCl powder. The purification was to remove the cupric ions present in the as-received CuCl powder and was conducted in a nitrogen-purged glove box to prevent subsequent oxidation of the cuprous ions. The purified powder was prepared by leaching and filtering. Leaching with 0.5 N HCl effectively removed any  $\text{CuCl}_2$  from the untreated CuCl powder. A quick check on the efficiency of the leaching was made by collecting 5 ml of the filtrate and adding 2 ml of 1.0 M sodium citrate. The presence of cupric ions in the filtrate was indicated by the formation of a light blue complex. After complete leaching, the CuCl was rinsed with acetone, dried, and then stored in dark, airtight bottles for later use.

The electrical characteristics of one of the best wet processed cell segments made using the above techniques is shown in figure 12. The cell was not completed in the usual sense in that it did not possess evaporated grids for the p contact. Instead, a gold metal mesh was pressed into contact with the barriered surface to obtain the readings. As evident from this figure, the wet processed cells displayed poor shunt as well as other characteristics that resulted in low efficiencies.



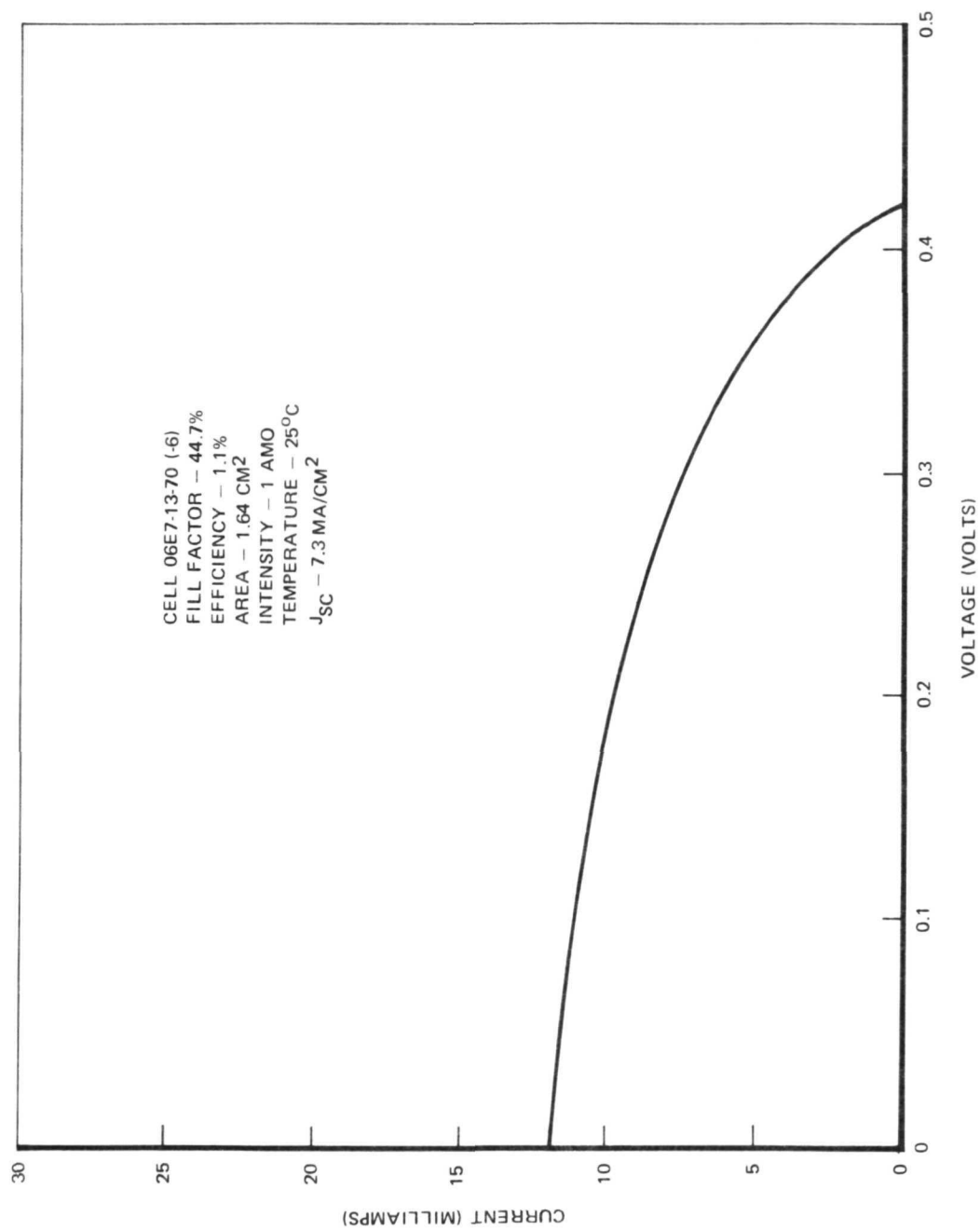


Figure 12. V-I CURVE OF A WET PROCESS CELL SEGMENT

## CELL FABRICATION---DRY PROCESS

Just prior to the midpoint of the second year's effort, the fabrication of cells by a dry process for barrier formation was initiated. There were a number of factors that motivated the development of an alternative method for barrier formation. Among these factors were: (1) the general interest of a single atmosphere (vacuum) cell fabrication process; (2) the demonstrated lack of reproducibility in the existing wet process; and (3) the relatively slow rate of progress possible towards improving the cell characteristics using the wet barrier.

Dry barrier processing was first accomplished on unetched CdS. The barrier was obtained by evaporating purified CuCl from a quartz crucible onto the unheated CdS substrate in a high vacuum, followed by an air bake at 180°C for 2 minutes. An example of the V-I characteristics of an unetched dry barrier process cell is shown in figure 13.

Subsequently, dry barrier deposition followed by a vacuum bake was also completed successfully. Although the temperature of the bake cycle went higher than intended, to 275°C, the cell had the highest conversion efficiency of any cell, wet or dry process, fabricated to that time. The V-I characteristics are shown in figure 14.

It was then found necessary on these initial samples to omit the etch step in the cell processing because of the high incidence of shorted cells. This was evident by the observed low  $V_{oc}$  values. It was later determined that the shorting experienced at that time was due to thin CdS (15 to 25 microns) rather than the intended 30 to 40 micron thickness. The cause of the discrepancy was the use of an uncalibrated crystal monitor. After correcting the monitor to obtain thicker CdS films, it was possible to consider an etch step in conjunction with the dry barrier formation.

Using the standard process bake parameters at that time (vacuum bake at 180°C for 4 minutes), but with three important additions, the most efficient cell segment of the entire program was fabricated (see Figure 15). A complete set of V-I curves, dark reverse and forward curves as well as illuminated power generation curves, are presented showing the excellent characteristics of the segment. The first addition was the cleaning of the cell in alcohol prior to etching. Because it was believed that a thin layer of sulfur was on the deposited CdS surface, both alcohol and carbon disulfide were used as solvents. As no visual differences were noted between films processed in these two liquids, for convenience reasons alcohol was selected for the solvent.

The second modification to the cell fabrication sequence was the application of a 4-second HCl etch (2:1 HCl: water) prior to the CuCl deposition. It is believed that the inclusion of this step was largely responsible for the marked improvement in conversion efficiency.

The third addition was omitting the aluminum p-contact bar that had been deposited on the p-contact edge of the cell. Instead, a conductive silver paint strip was applied in the middle of the cell across the gold grid lines. This greatly reduced the series resistance apparent in earlier V-I characteristics of nonshorted cells.

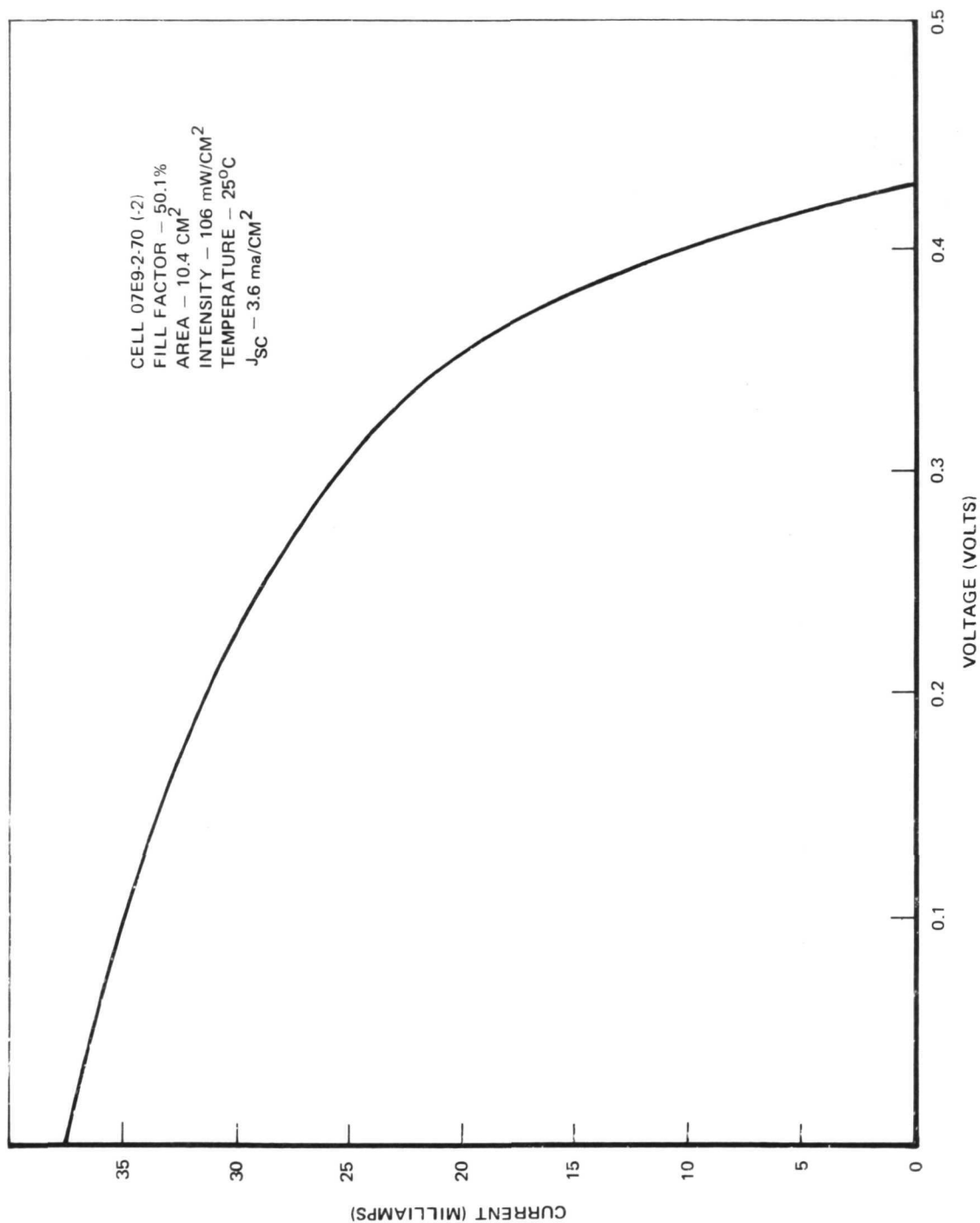


Figure 13. V-I CURVE OF AN UNETCHED DRY PROCESS CELL SEGMENT

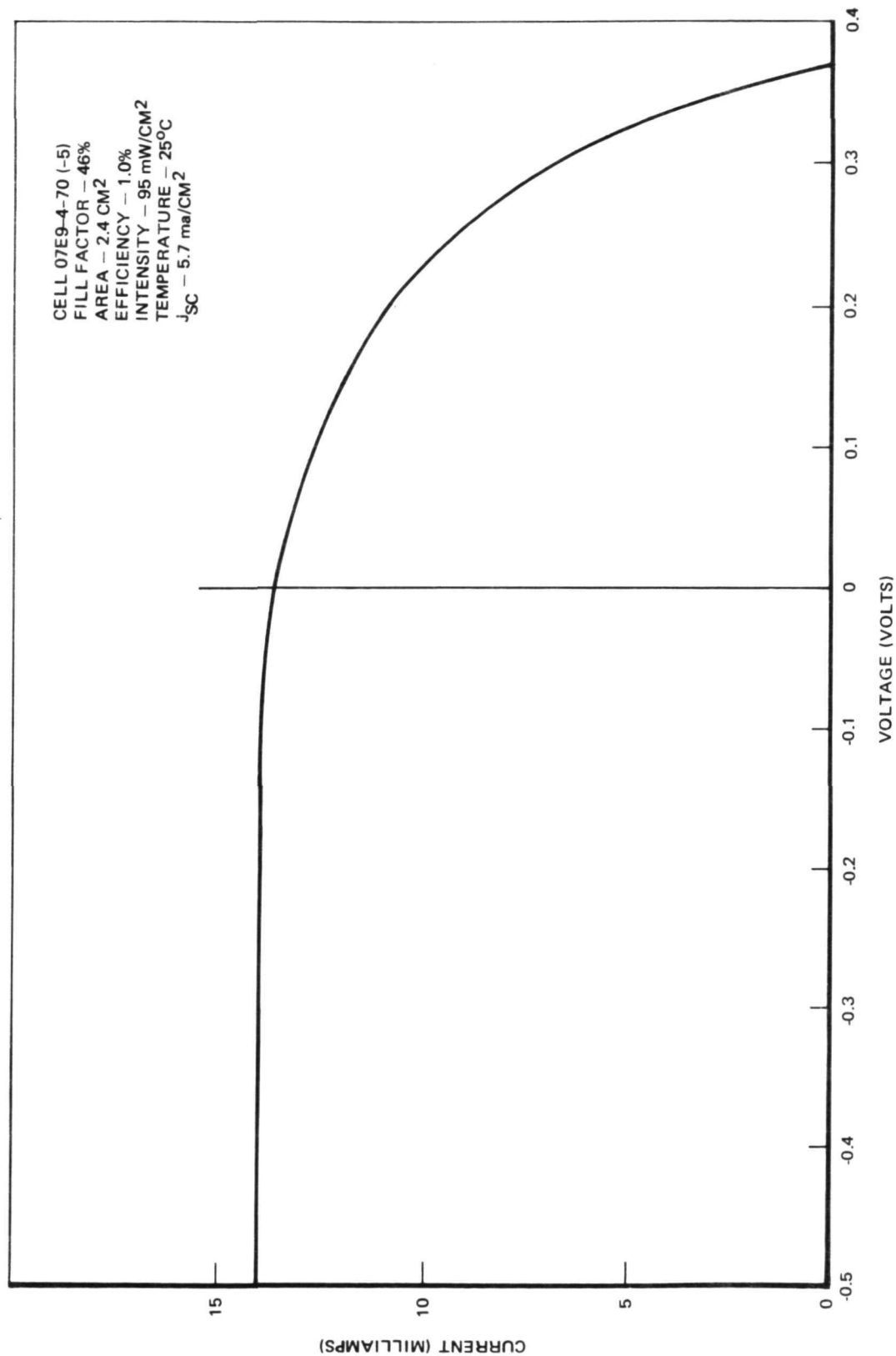


Figure 14. V-I CURVE OF AN UNETCHED VACUUM BAKE DRY BARRIER CELL SEGMENT

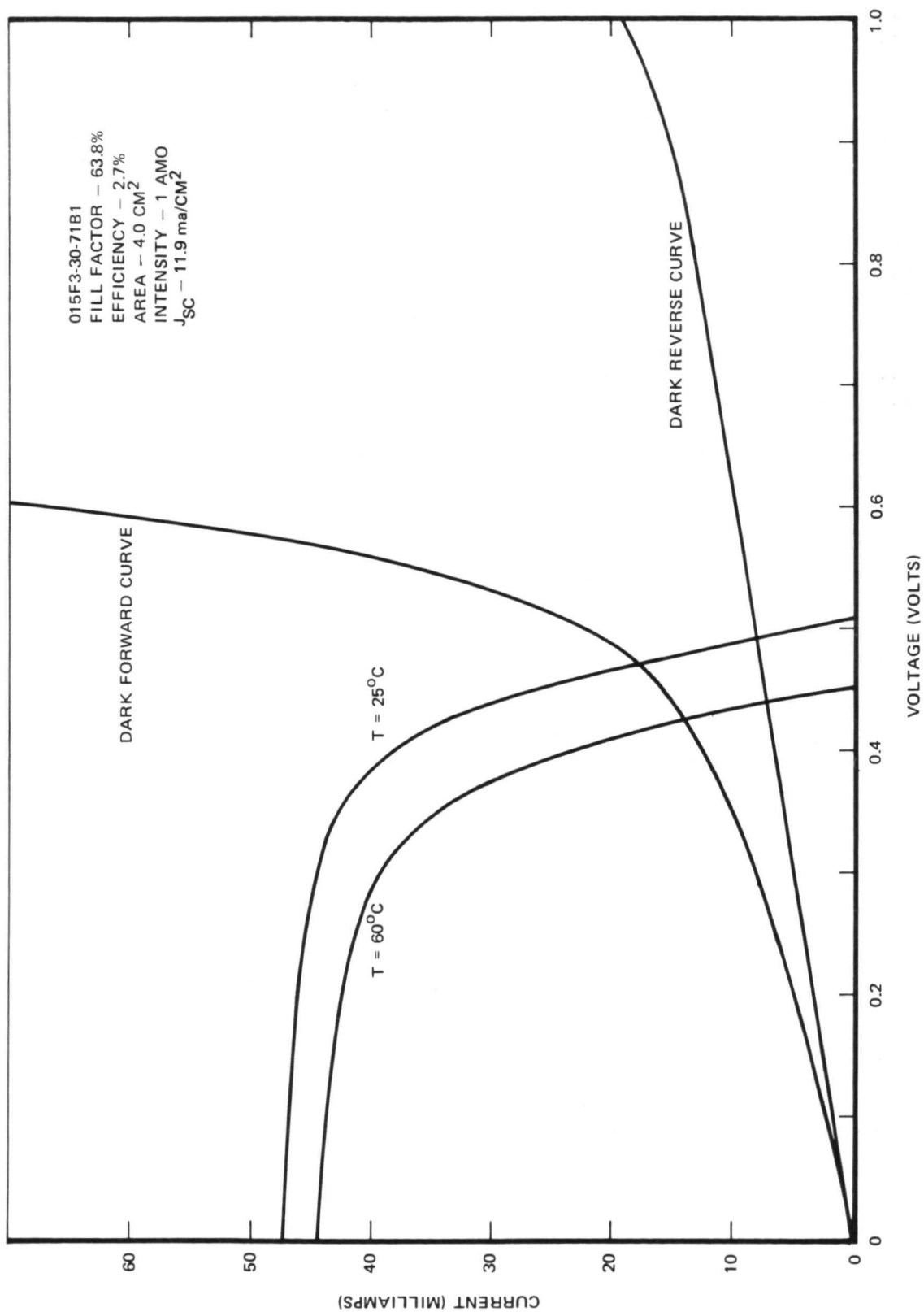


Figure 15. V-I CHARACTERISTICS OF AN ETCHED DRY PROCESS CELL SEGMENT

The use of this paint necessitated however, adding a 4-minute air bake for properly curing to achieve a low resistivity. This processing yielded cells with an open-circuit voltage greater than 0.5 volt.

Figure 16 shows the V-I curve of a cell, 015F4-29-71B which had a copper wire adhered to the cell surface with gold filled epoxy. The gold filled epoxy took quite long to cure, overnight at 100°C, but a higher current was subsequently obtained. The cell showed a short-circuit current of 350 ma; a current density of 11.7 ma/cm<sup>2</sup>, the best of any complete cell.

To optimize the bake following the CuCl evaporation step, a parametric study was undertaken. The matrix of bake parameters was as shown in table II, with a sample being run at each condition. Following each bake condition samples had gold grids deposited and in turn had silver paint applied across the grids for the top p-contact. Voltage-current (V-I) data were obtained after a short room temperature drying of the silver paint, after a 2-minute air bake at 250°C and again after a second 2-minute air bake at 250°C. Voltage-current curves for the samples are shown in figures 17(a) through (h). Curves for the series A segments were so low that they were recorded only after receiving the first air bake.

TABLE II  
MATRIX OF BAKE PARAMETERS

Temperature °C		180			250		
Time Minutes		4	8	16	4	8	16
Environment	Vacuum	A1	A2	A3	A4	A5	A6
	Air	B1	B2	B3	B4	B5	B6
	H <sub>2</sub>	C1	C2	C3	C4	C5	C6
Samples were from submodule 017F5-12-71							

While there are a number of inconsistencies apparent in the V-I curves, they do show the desirability of using low temperatures and short times for the CuCl bake operation. This set of samples also appears to indicate that an air environment during the bake (B-series) was superior to vacuum or hydrogen. Because of the obvious shunting problem associated with the cells, the significance of this last observation is questionable.

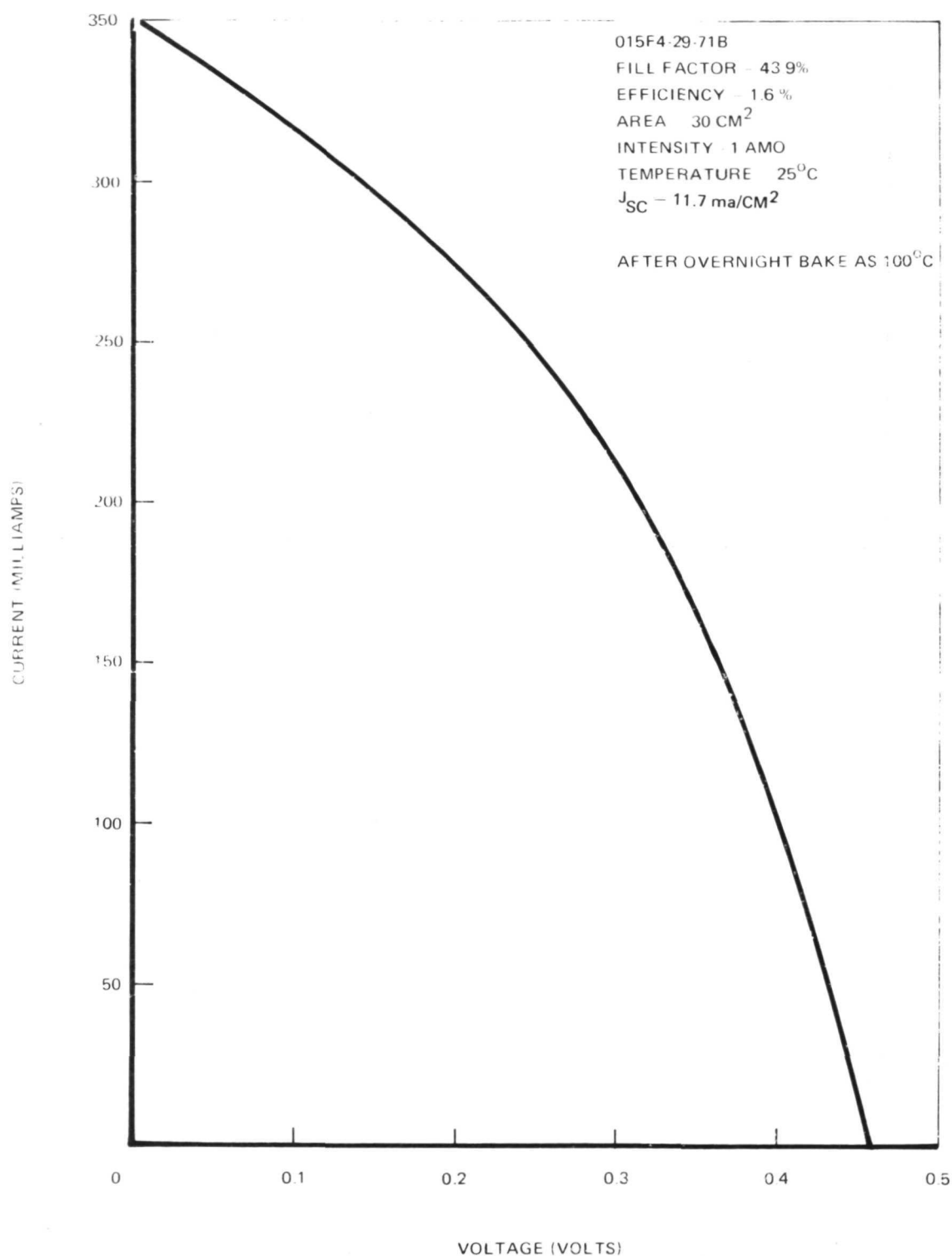


Figure 16. V-I CHARACTERISTIC OF COMPLETE CELL

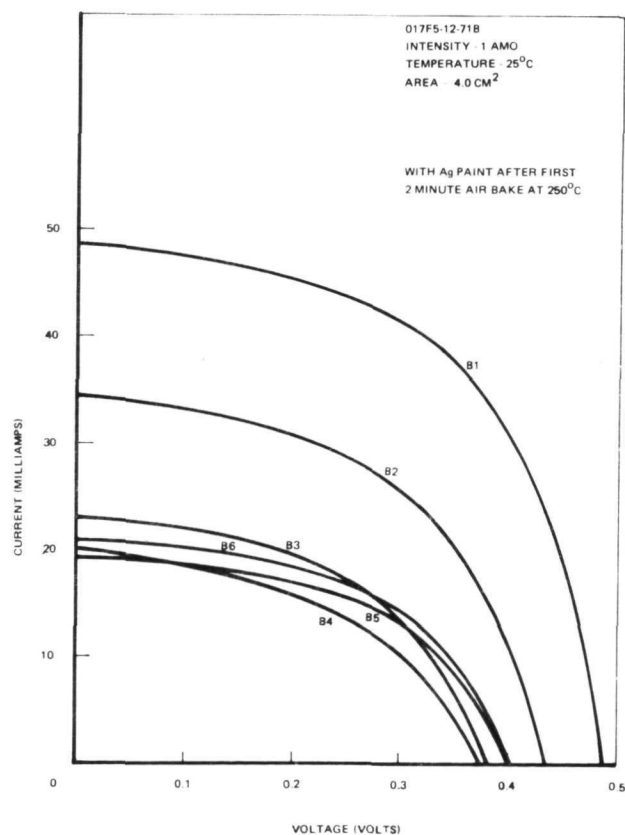
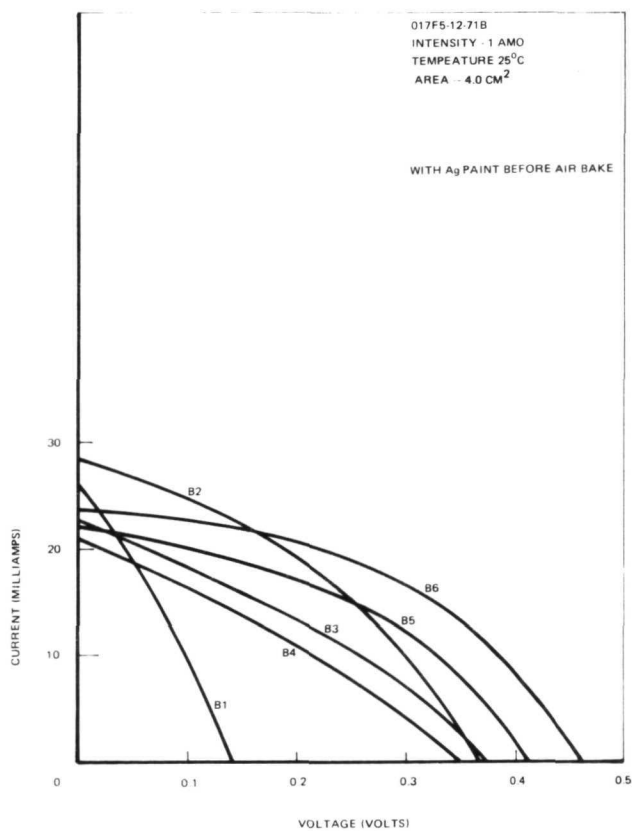
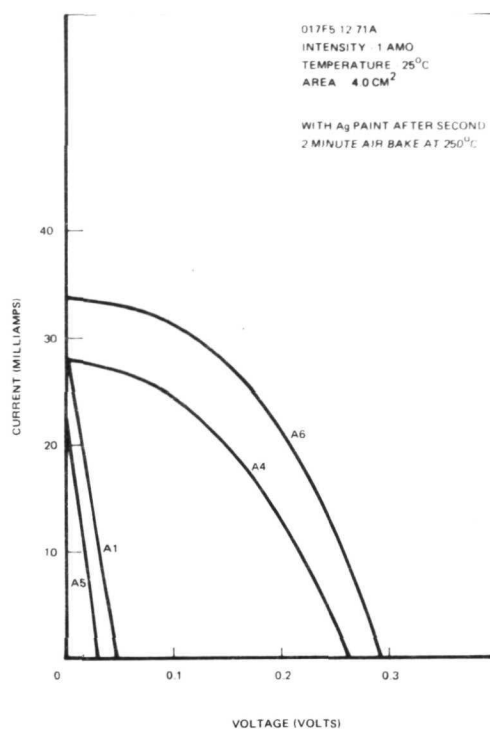
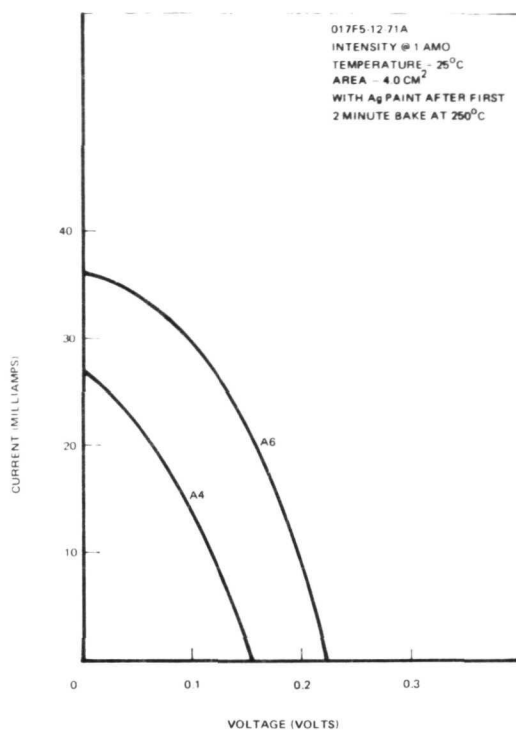


Figure 17: V-I CHARACTERISTICS OF SAMPLES DESCRIBED IN TABLE II



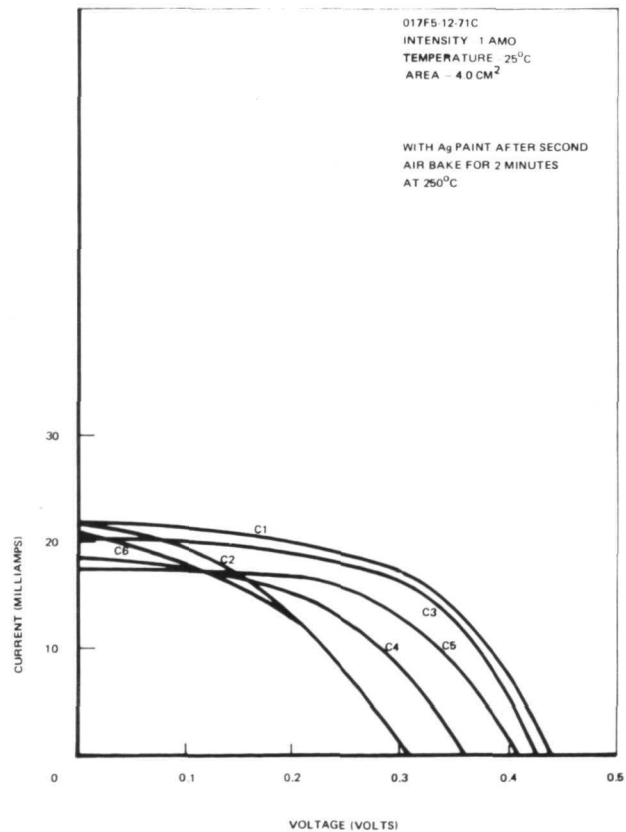
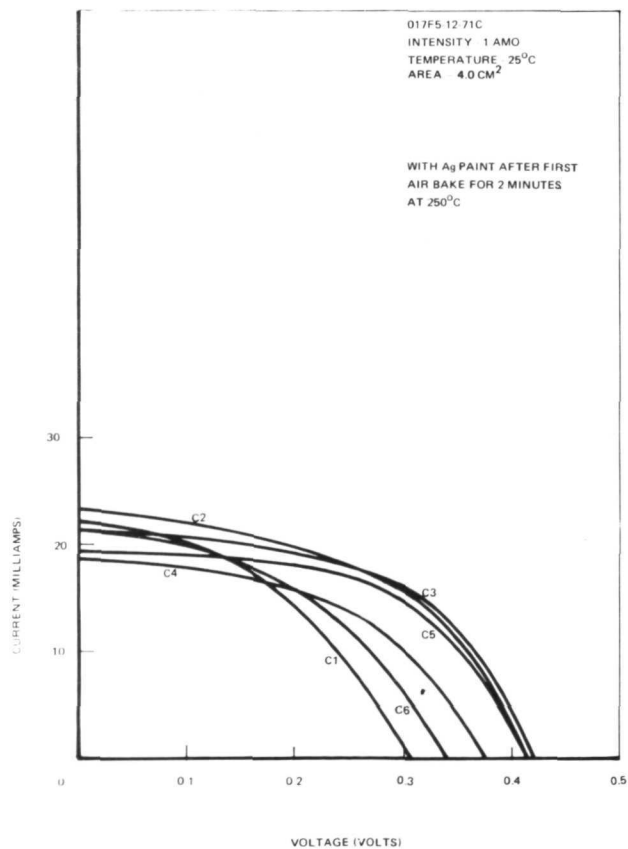
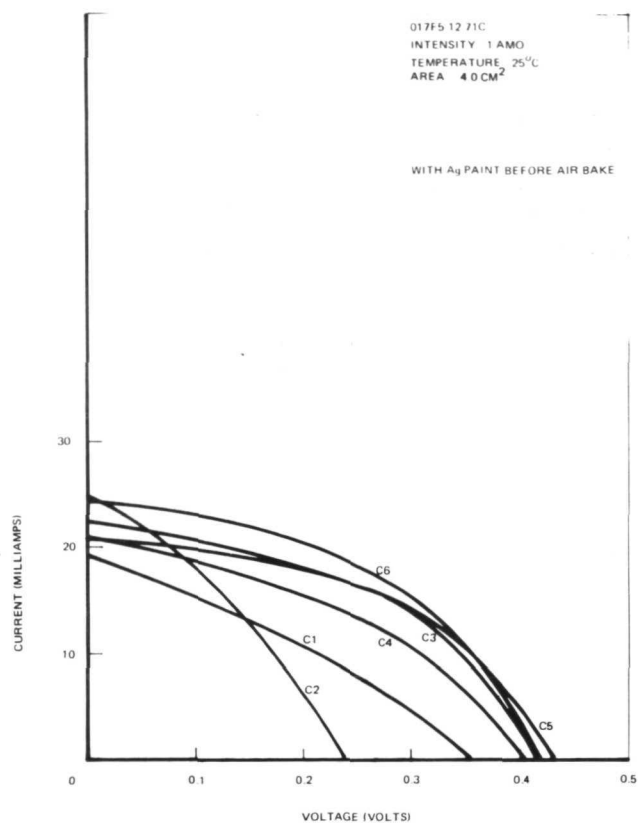
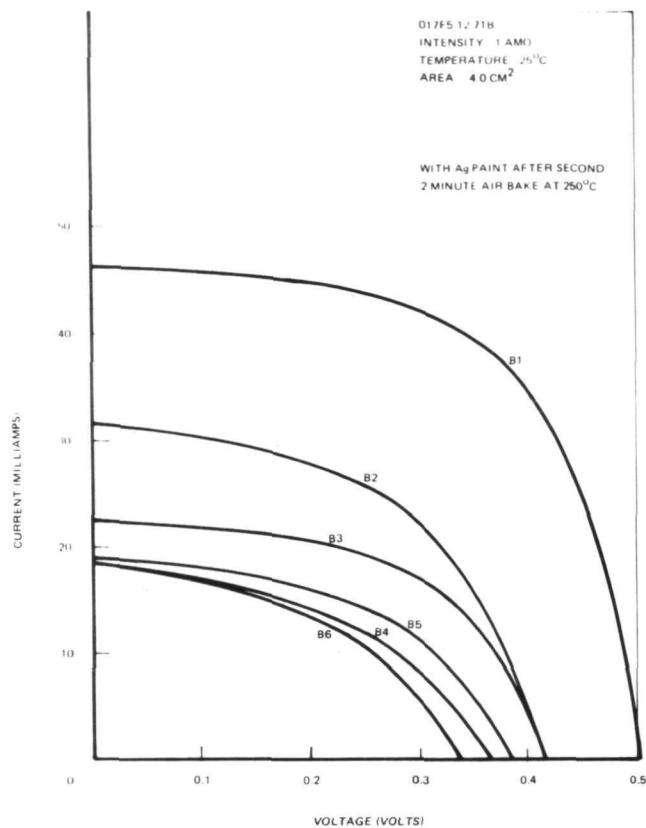


FIGURE 17 (CONTINUED)

The effect of an air bake following the grid deposition was to increase the  $V_{oc}$  and square up the V-I curve. This behavior was common to all of the samples and had been encountered with earlier cells. After the short air bakes, the conversion efficiencies for the best samples were in the 2.1 to 2.4 percent range. After analyzing the V-I curves, it was decided to conduct a portion of the tests again. A matrix as shown in table III was established. Segments had gold grids and silver paint applied to them for contacts. Figures 18(a) and (b) show the V-I curves for these samples before and after a 2-minute air bake of 250°C.

TABLE III  
MATRIX OF BAKE PARAMETERS

		180°C	
Environment	Time Minutes	4	8
	Vacuum	A1	A2
	Air	A3	A4
	H <sub>2</sub>	A5	A6

Samples were from submodule 017F5-14-71

In this series, the hydrogen bake environment was clearly shown to be superior, with reasonably good characteristics being obtained even before baking in air. Baking in air tends to reduce the differences between the various samples but the hydrogen cells remain superior. The air bake again generally shows an increase in  $V_{oc}$  and in the fill factor but a loss in short circuit current. The best efficiencies for these cell segments were 2.1 to 2.4 percent.

#### SPECTRAL RESPONSE

Spectral response for two cell segments are shown in figures 19 and 20. It is to be noted that the relative heights have no relationship to each other as our data reduction allowed only for normalization of each curve to its own data. It should further be noted that no light biasing was used in these spectral response measurements. Nevertheless, the data for segment 015F-3-30-71B1 shows a significantly greater long wavelength response in comparison to segment 014F3-12-71A3. This difference is attributed to the processing. The major processing difference between these two samples was the fact that the first sample was unetched while the latter cell was given a 4-second etch in 2:1 HCl: water prior to barrier formation. The large improvement in long wavelength response gives rise to a much higher conversion efficiency, i.e., <1 percent versus 2.7 percent.

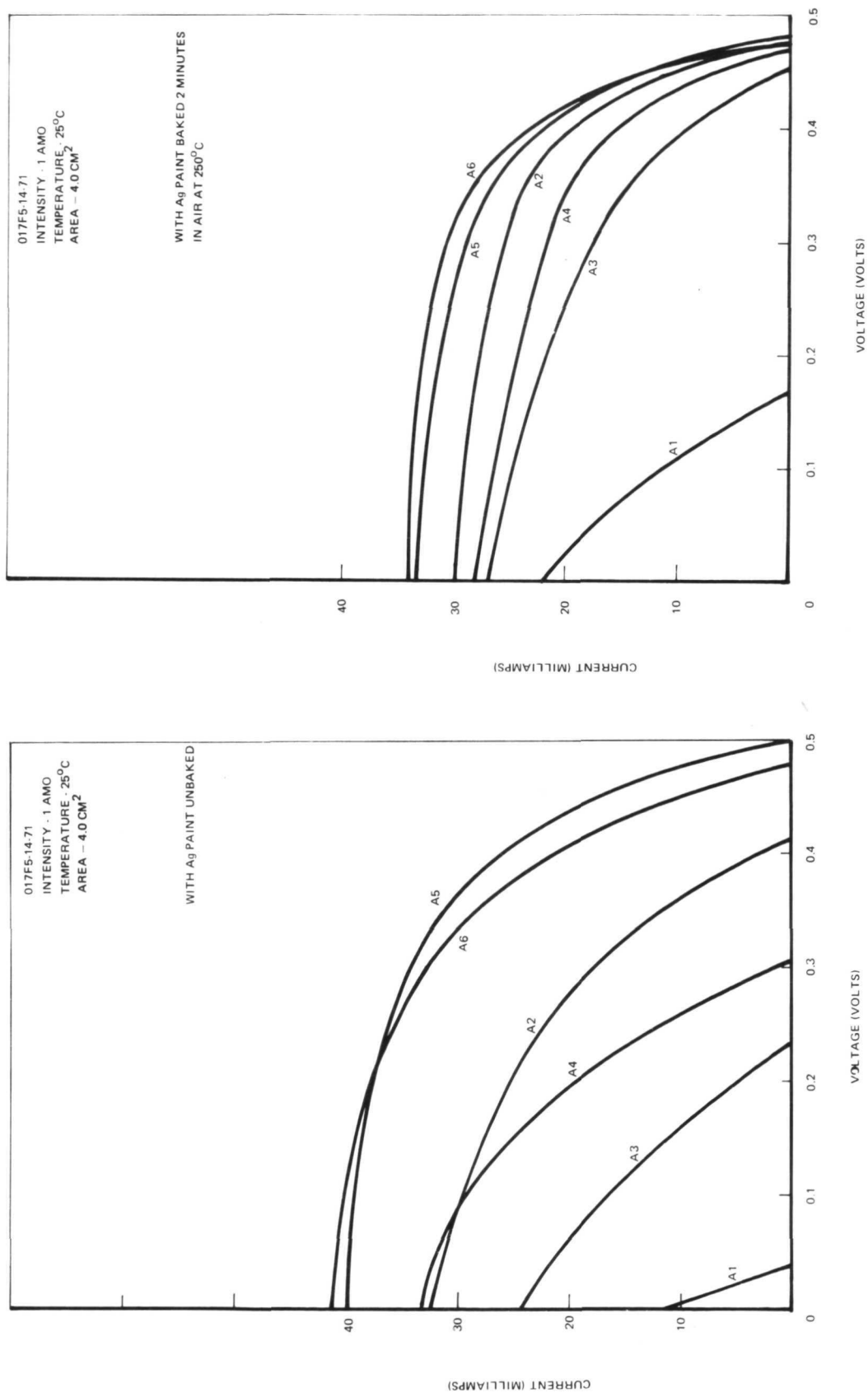
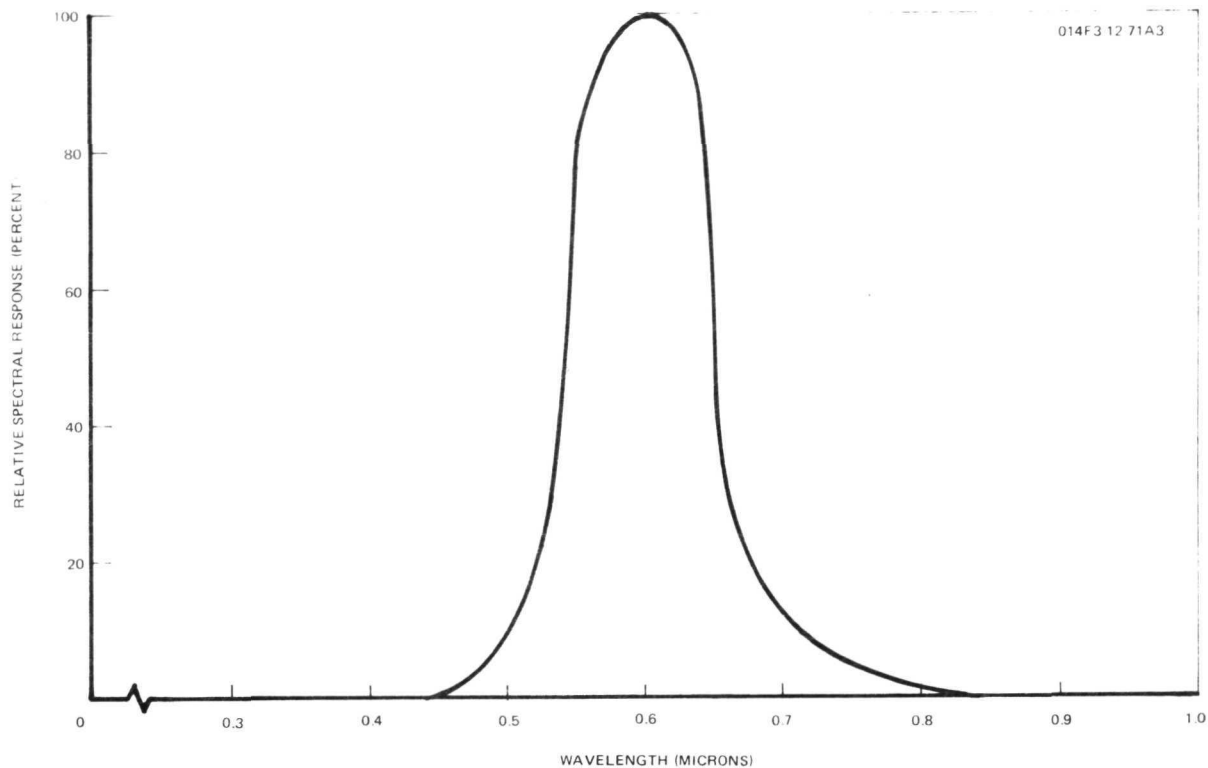
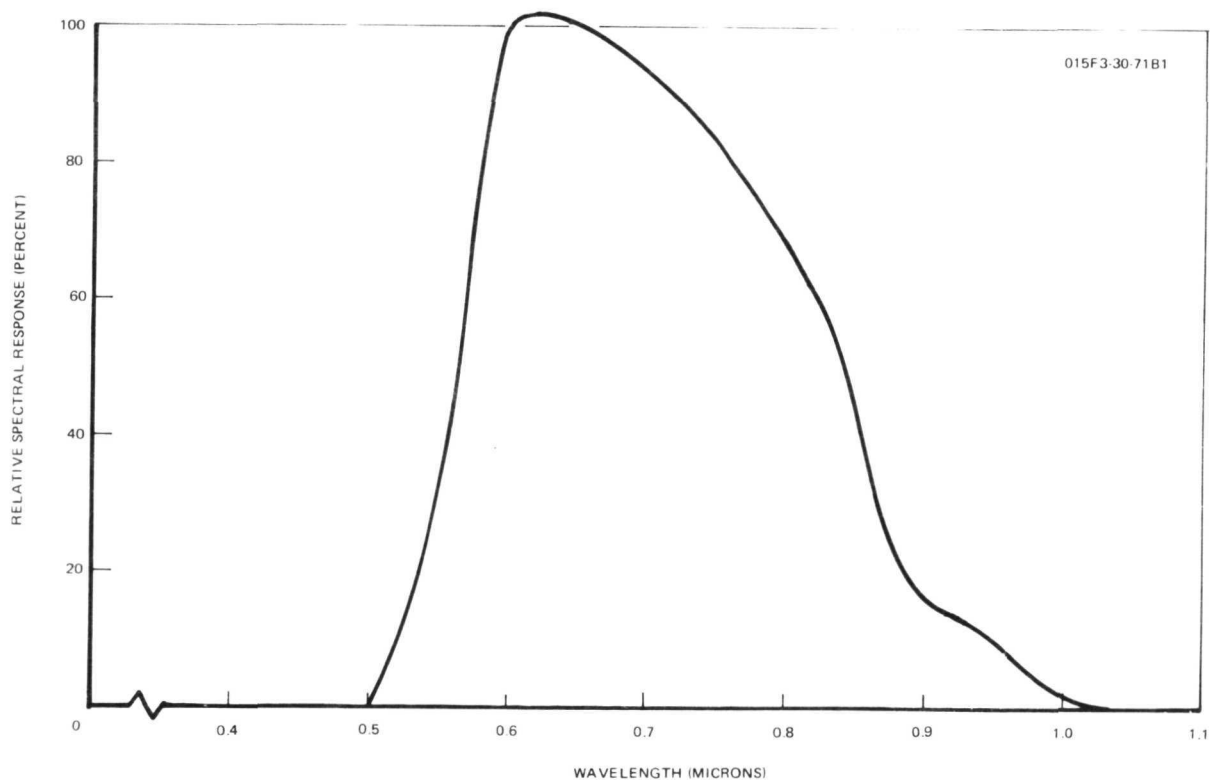


Figure 18: V-I CHARACTERISTICS OF SAMPLES DESCRIBED IN TABLE III



*Figure 19: SPECTRAL RESPONSE (WITHOUT BIAS LIGHT) OF UNETCHED CELL SEGMENT*



*Figure 20: SPECTRAL RESPONSE (WITHOUT BIAS LIGHT) OF ETCHED CELL SEGMENT*

## Encapsulation of the CdS Solar Cell

Several adhesives for use with a cell cover plastic, 1-mil kapton, were investigated. A Hysol polyamide epoxy was used to successfully bond kapton to the CdS, but air pockets formed under the cover plastic. Also, Schjeldahl GT-100 polyester resin, in tape form, was used to bond kapton to the CdS, but resulted in a poor bond. It was later found that the bonding pressure used for these tests was too high and applied for too long a period of time.

Following these initial attempts at selecting a suitable adhesive, the investigation then considered (1) GT-100-coated kapton; (2) astro-epoxy-coated kapton; and (3) a silicone, R63-488, as an encapsulant. While poor adherence was obtained with the GT-100-coated kapton, both the astro-epoxy-coated kapton and R63-488 appeared to adhere well enough to subject them to a 5-cycle thermal shock test. This consisted of being held for 2 minutes at either +124°C or -196°C (liquid nitrogen) then immediately transferring the cell to the other temperature. Both materials appeared to hold up well. A loose corner of the astro-epoxy-coated kapton was found, however, and the kapton easily peeled away from the adhesive. The silicone was found to have excellent adherence and no curling of the substrate due to the silicone was apparent. Accordingly, the R63-488 was used in subsequent encapsulations of cells.

## Isolation Strip Materials

An isolation strip of  $\text{SiO}_x$  was originally deposited over the edges of the CdS film before the etch step and other wet processing. But cells appeared to short frequently. Even after the implementation of the dry process barrier formation, a thin  $\text{SiO}_x$  isolation strip (0.5 micron) was deposited prior to the HCl etch step. Cells continued to short. Thin depositions of  $\text{SiO}_x$  were made before the etch step and following the dry barrier processing, but shorted cells persisted.

A study of the shorting modes of the cells indicated that the shorting took place at the metallization tab deposited on the thin  $\text{SiO}_x$  crossing over the CdS edge at the gap. The  $\text{SiO}_x$  seemed to crack and peel following immersion in the acid etch solution. This was particularly evident in the CdS edge region where the  $\text{SiO}_x$  was extremely thin. It was decided to investigate plastics that would be impervious to the acid solution and thicker for better electrical isolation, yet easily applied and permanently flexible consistent with the overall design of the solar cell.

Materials investigated were the silicones Sylgard 184 and 186, and Pyre ML varnish---liquid kapton. Sylgard 184 was used with a Sylgard primer, which allowed the silicone to adhere well but to spread some before curing. Sylgard 186, supposedly more viscous than 184, was initially applied without the primer, but it spread some and also had poor adherence; a primer was therefore necessary.

The silk screening method was selected for applying the plastics, therefore, the more viscous material was desirable. Sylgard 186 was silk-screened onto a primed surface and adhered well with a minimum of spreading. When the plastics were initially considered, they were to be used only under the six crossover tabs, but because the  $\text{SiO}_x$  continued to crack and chip under the contact bar on top, this design was replaced with total edge protection. The edge-protection design was revised from the initial design of being only over the CdS 15 cm edges to include the total edge so that the top surface was "boxed" in. All indications were that the use of Sylgard 186 eliminated the shorting taking place at the crossover tab of the p-contact.

Pyre ML varnish, also investigated, could be brushed on well, but did not silk-screen well, so was not considered further as an isolation material.

Because of the interest in locating the shorting taking place in the cell, a technique was borrowed from microcircuit failure analysis for locating the shorts. This technique, which involved submerging the cell in Freon and applying voltage across the electrodes with probes, was successfully applied to a shorted CdS solar cell. As a result of heat generated at a short, small bubbles formed in the Freon, showing the short location. The bubbles were visible under a microscope, and often with the naked eye.

#### Submodules

The concept of fabricating interconnected cells into submodules using thin-film integrated circuit technology was shown to be valid. Typical V-I characteristics for 3-cell submodules as developed in this program are shown in figures 21 and 22. The initial design utilized  $\text{SiO}_x$  deposited in the isolation strip of the p-contact bar/crossover tabs and the  $\text{CdS}$ . But as the fabrication processes for the cells developed, mainly using an HCl etch to achieve higher output cells, it was found that the  $\text{SiO}_x$  cracked, chipped, and delaminated, allowing the cell to short when the p-contact bar was deposited.

As described in the previous section, a silicone Sylgard 186, was used successfully in replacing the  $\text{SiO}_x$  for protecting the CdS edges during etching and contact evaporation. However, the silicone was much more flexible in the isolation gap than the  $\text{SiO}_x$  and allowed flexure of the crossover tabs. The crossover tab design was sufficient in current carrying capacity but its mechanical strength was insufficient to stand the flexing imposed by the soft silicone---thus it opened and electrical continuity was lost upon handling the modules.

Although no development time was spent on it, a glass resin was discovered that would seem to be a possible solution to the problem. Owens-Illinois glass resin polymer, Type 650, which is a material between silicones and glass, when composited with inorganic filler is said to offer excellent high-temperature electrical properties. At the same time it should be a firm base for the metal film depositions. This glass resin polymer should be tested and evaluated in the same manner as the silicones.

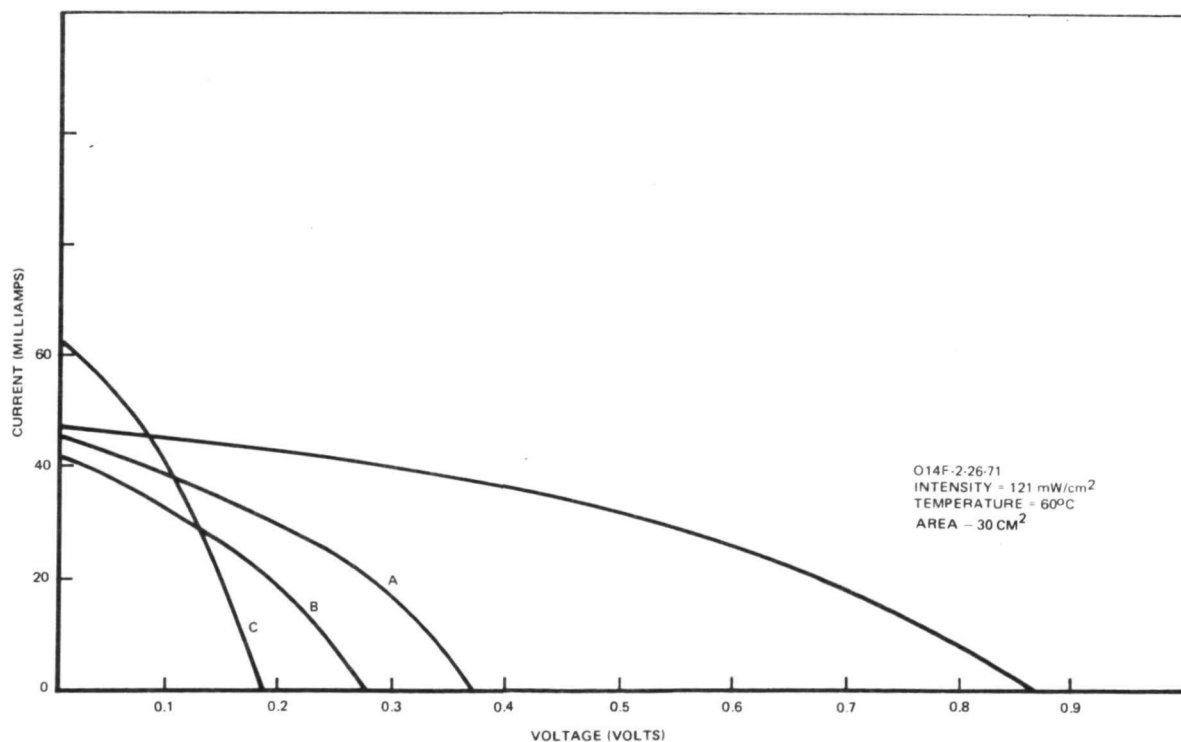
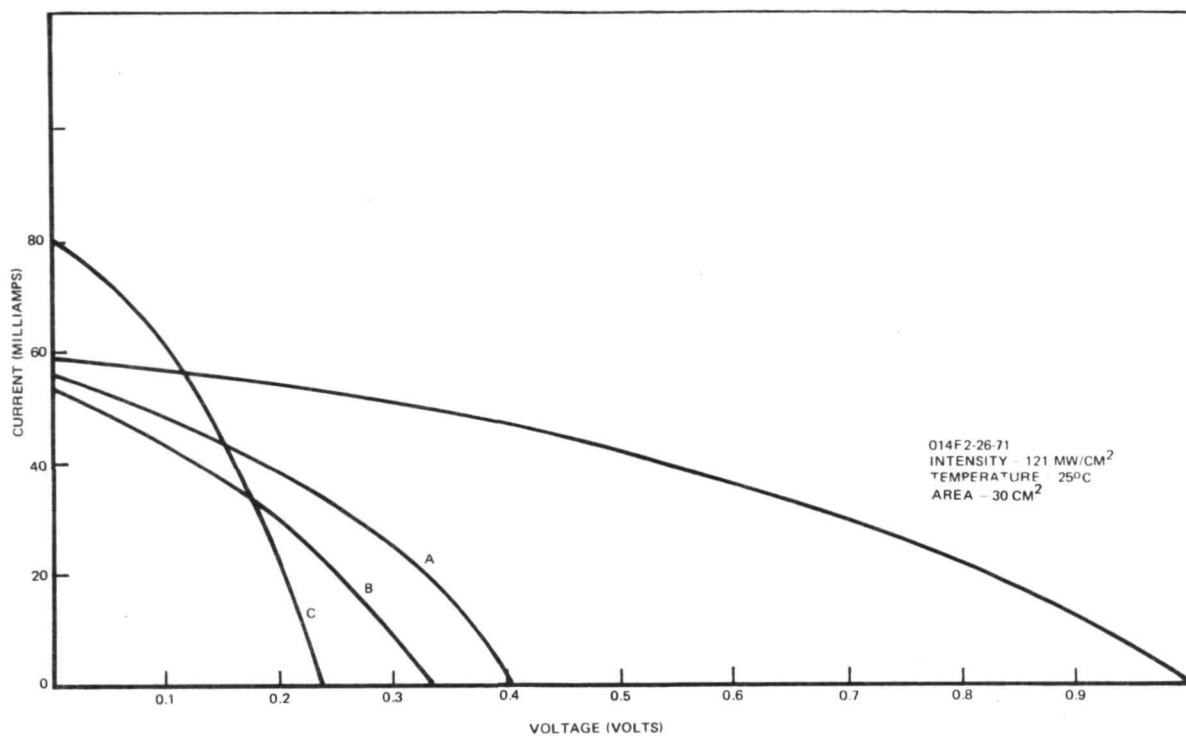


Figure 21: V-I CHARACTERISTICS OF SUBMODULE 014F2-26-71

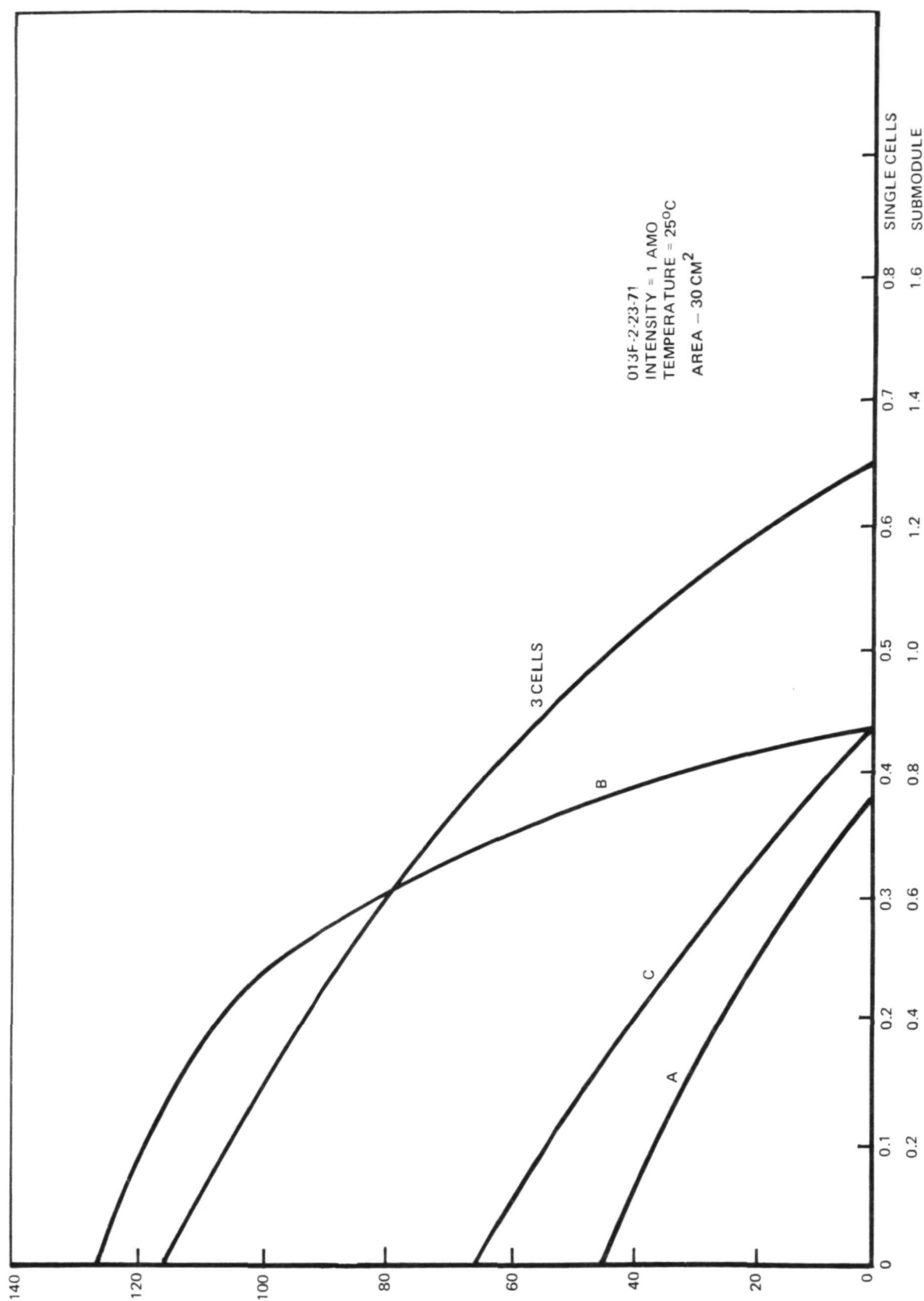


Figure 22. V-I CHARACTERISTICS OF SUBMODULE 013F2-23-71



## ANALYTICAL STUDIES

Several analytical studies were conducted to relate, if possible, the material characteristics to the solar cells performance. The studies, which were concentrated on the CdS and barrier layers, utilized specialized analytical instrumentation that may have value in future programs requiring characterization of material properties.

### Scanning Electron Microscope

The SEM was routinely used as an analytical tool during the course of the program. It was found to be especially effective in understanding the results of varying processing conditions on the cell performance. That is, a surface structure examination was often found to be of considerable value in making the correlation between process step and cell characteristics.

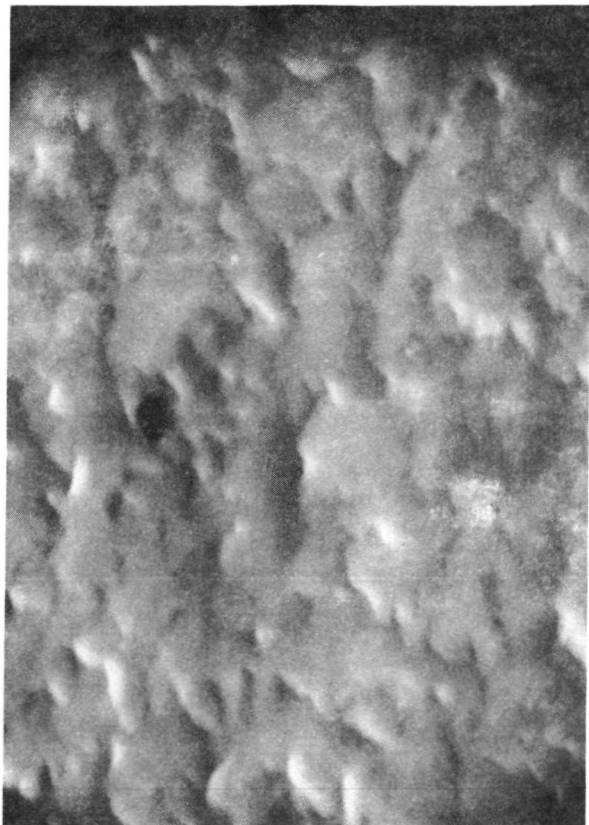
One of the initial studies made with the SEM was a comparison between the structure of CdS films deposited onto three different substrates. The effects of CdS powder preparation techniques and post deposition etching of the CdS films were also included in this study. Table IV lists the experimental conditions for the samples.

TABLE IV

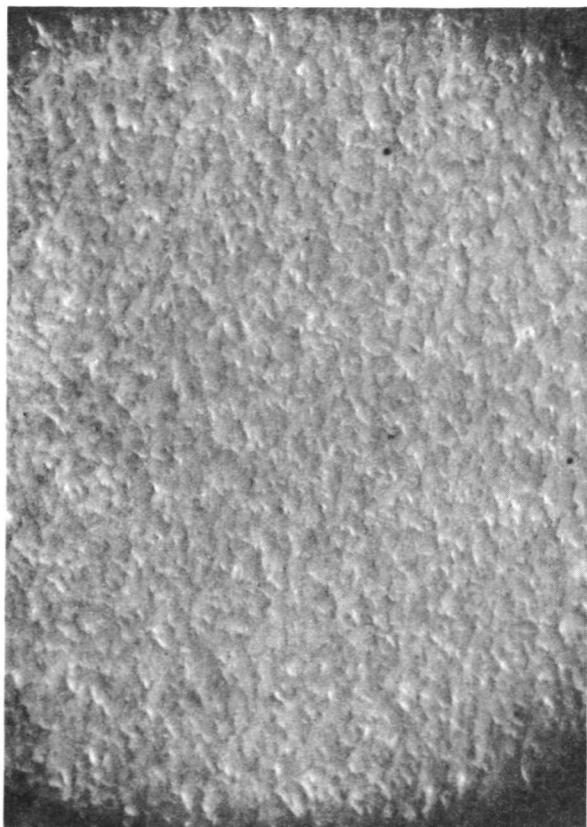
Experimental Conditions for SEM Test Samples

<u>No.</u>	<u>CdS Powder Preparation</u>	<u>Substrate</u>
1	6 hours at 700°C in vacuum followed by 4 hours at 1100°C in argon	Vacuum metallized kapton
2	64 hours at 800°C in argon followed by 8 hours at 1200°C in argon	Vacuum metallized kapton
3	Same as (2)	Molybdenum foil (Lewis supplied sample)
4	Unknown	Zinc plated, silver flake pigmented varnish applied to kapton (Clevite standard cell provided by Lewis)

All of the samples were examined in the unetched state and after a 2 sec etch in 3:1 HCl:water solution. The photographs presented in figures 23 through 26 are the results of the SEM study.



4500X

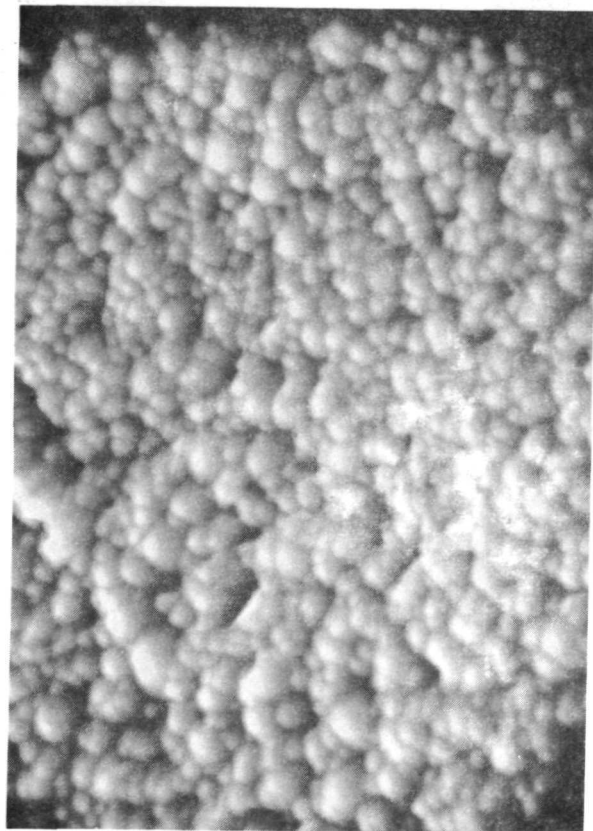


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230X

Figure 23(a): SEM PHOTOGRAPHS OF UNETCHED CdS  
FILM NO. 1 OF TABLE IV



4800X

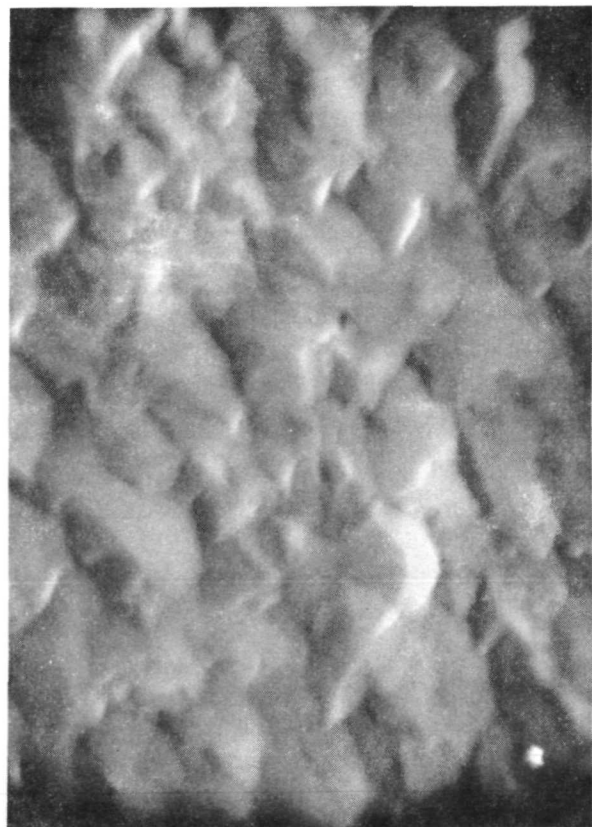


960X

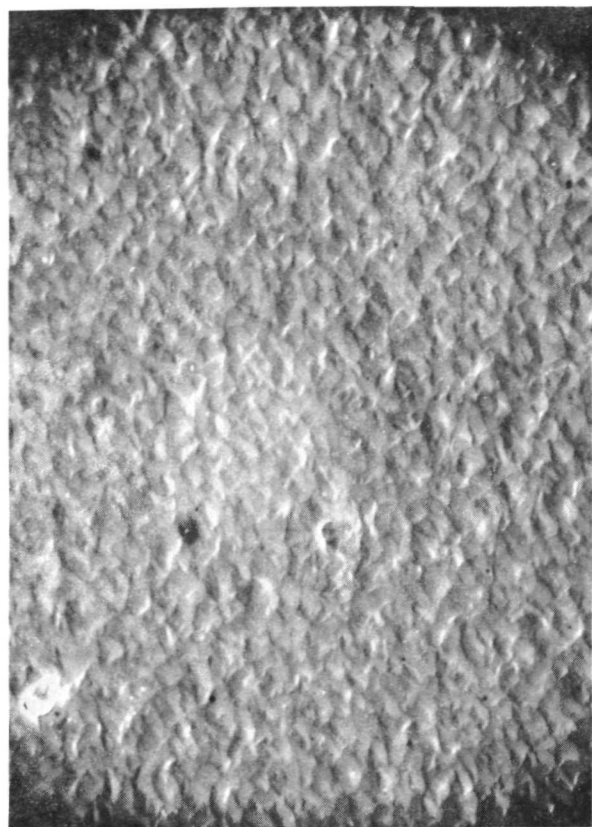


240X

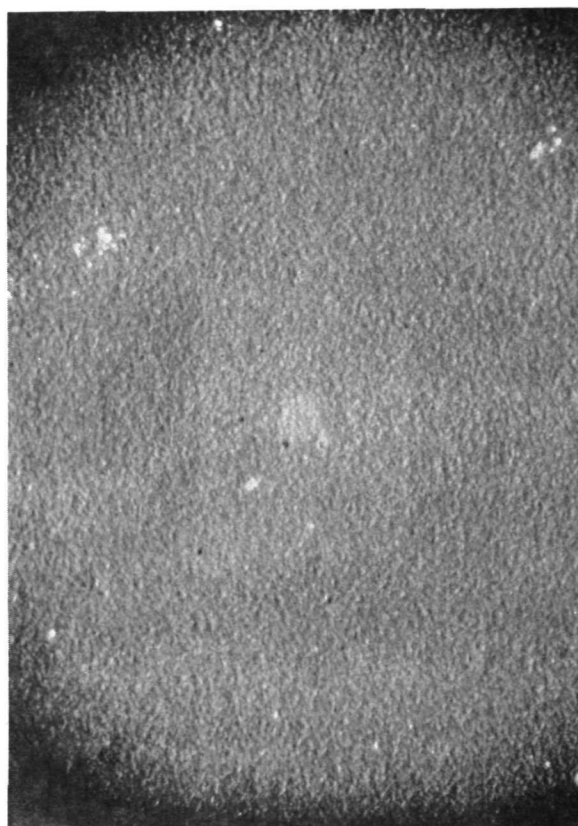
Figure 23(b): SEM PHOTOGRAPHS OF ETCHED Cds  
FILM NO. 1 OF TABLE IV



4600X

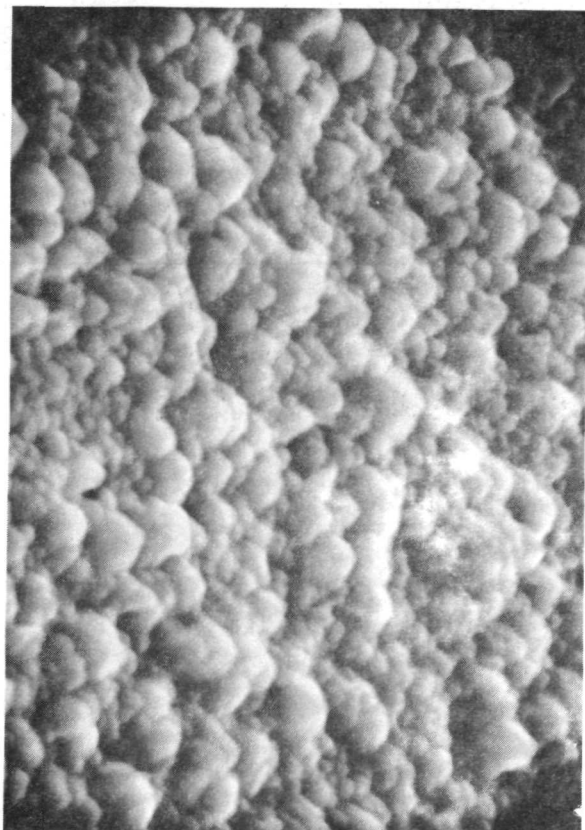


920X

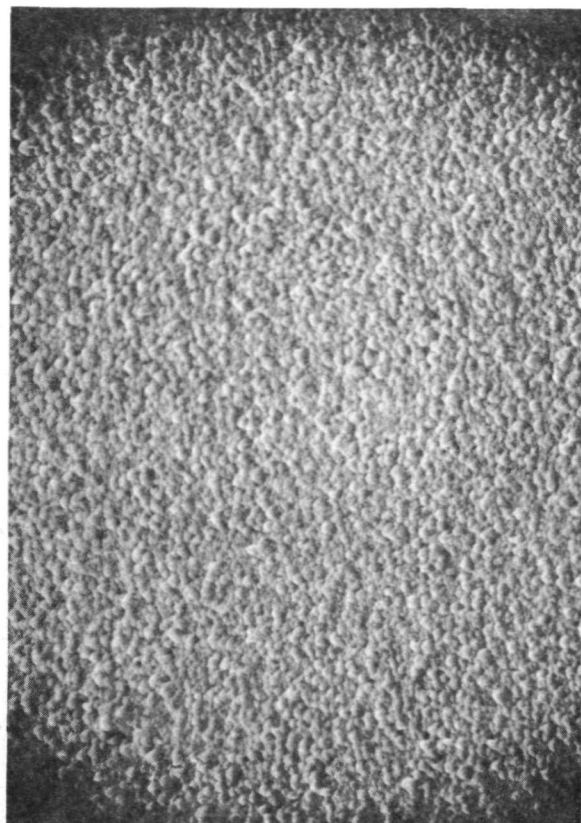


230X

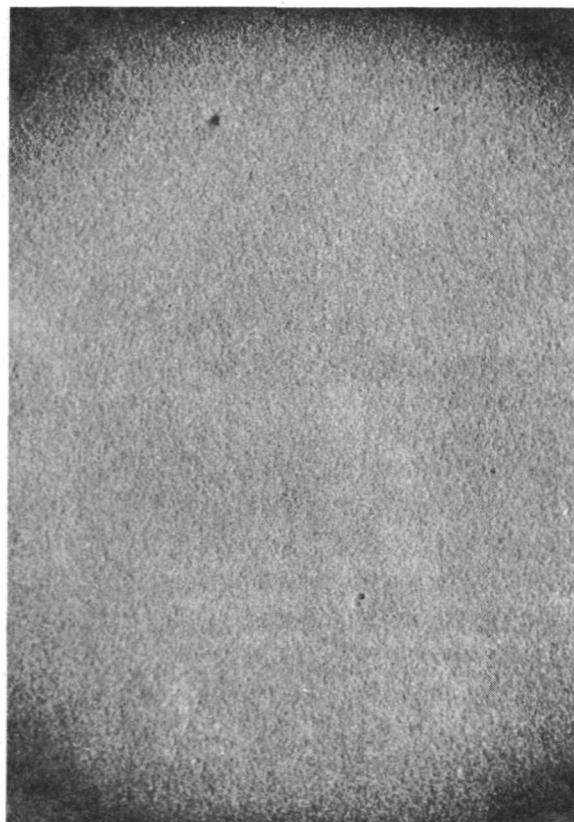
Figure 24(a): SEM PHOTOGRAPHS OF UNETCHED CdS  
FILM NO. 2 OF TABLE IV



4600X



920X



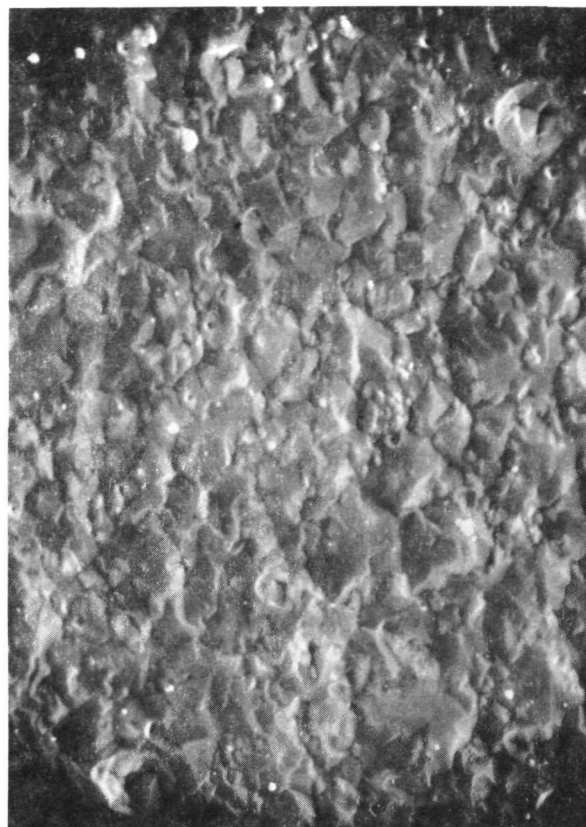
230X

Figure 24(b): SEM PHOTOGRAPHS OF ETCHED CdS  
FILM NO. 2 OF TABLE IV

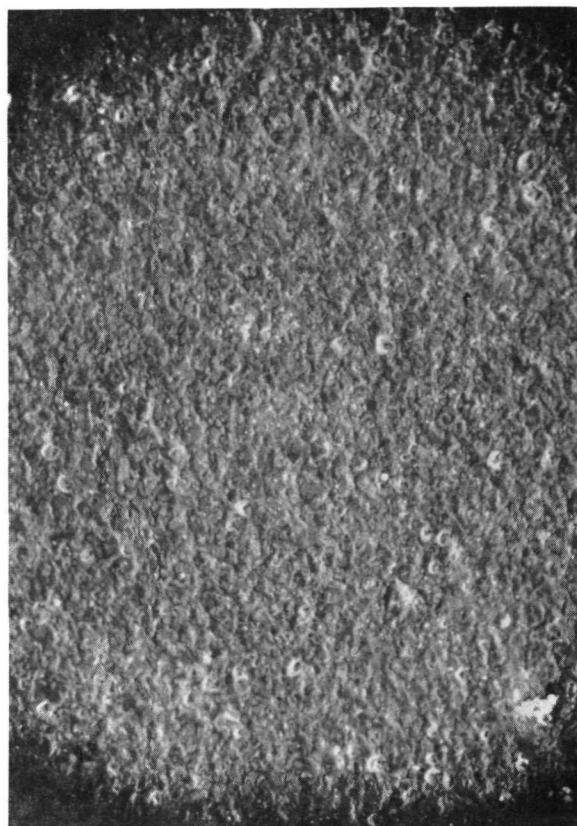




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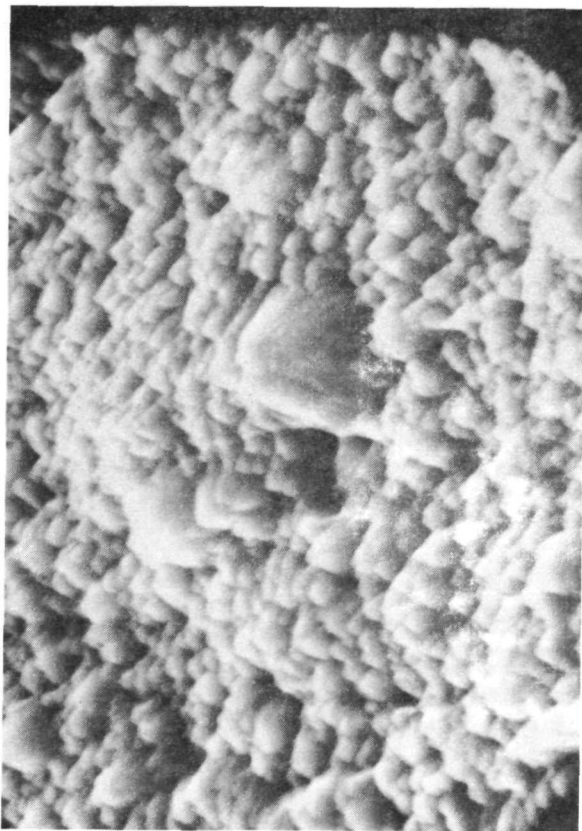


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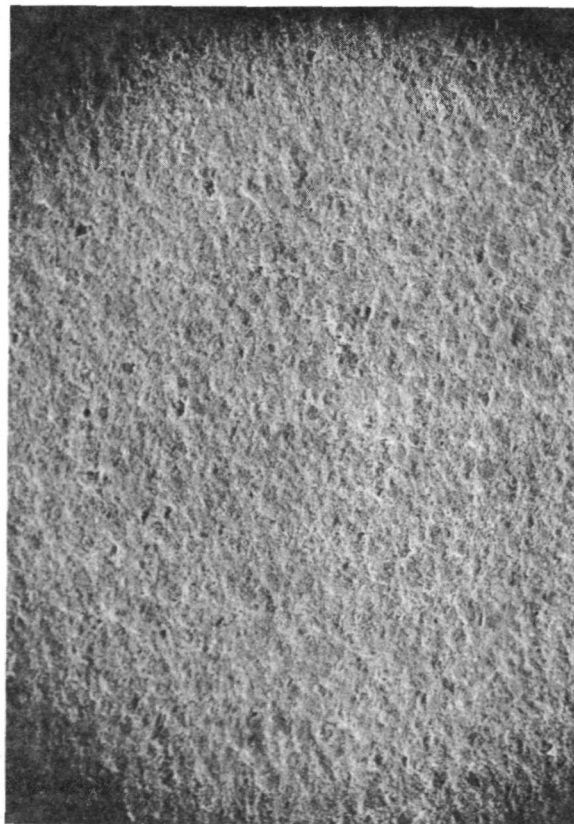
Figure 25(a): SEM PHOTOGRAPHS OF UNETCHED CdS  
FILM NO. 3 OF TABLE IV



4600X

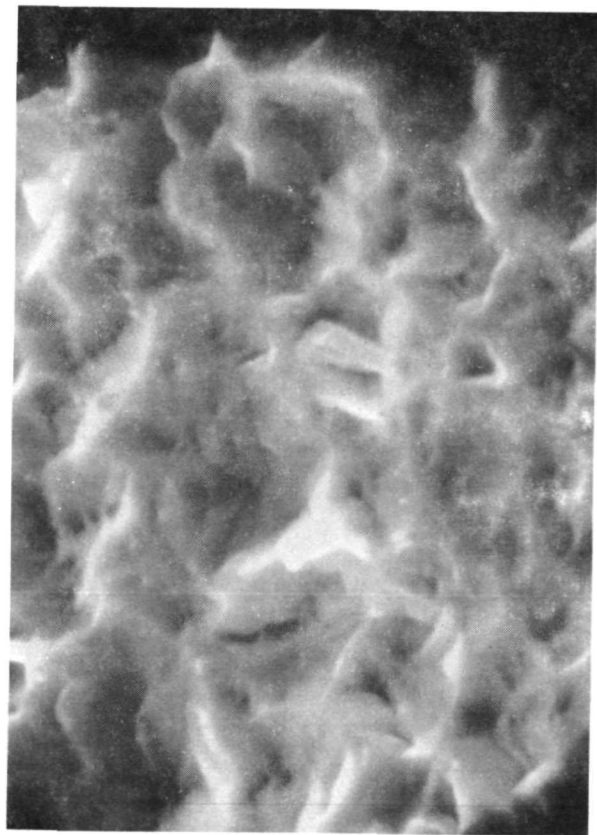


930X

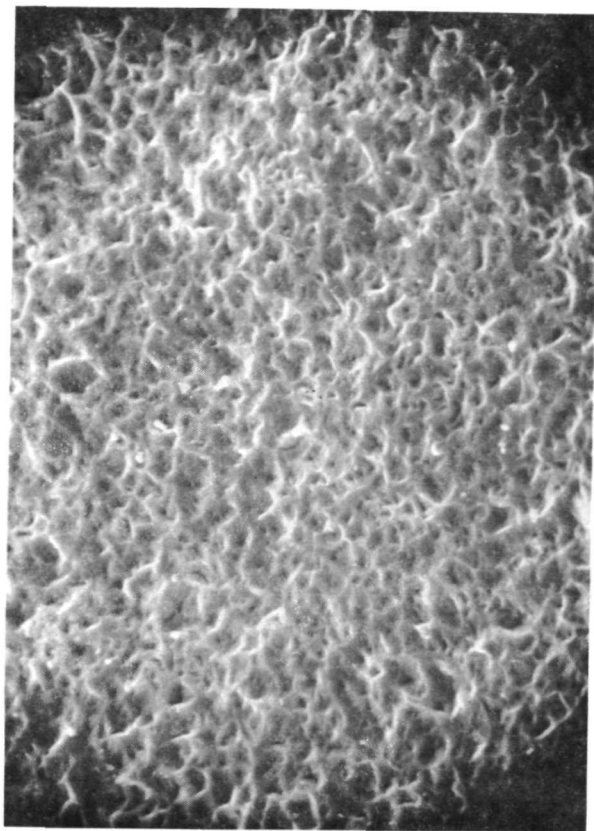


230X

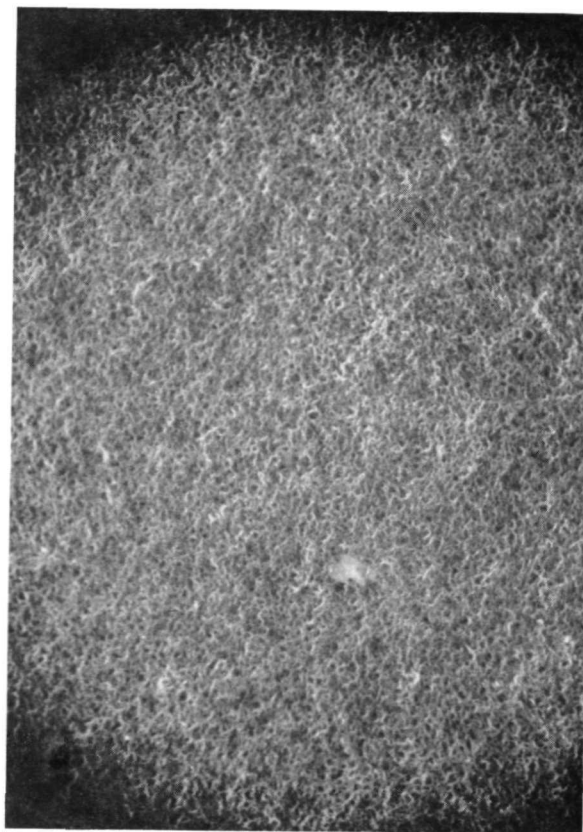
Figure 25(b): SEM PHOTOGRAPHS OF ETCHED CdS  
FILM NO. 3 OF TABLE IV



4700X



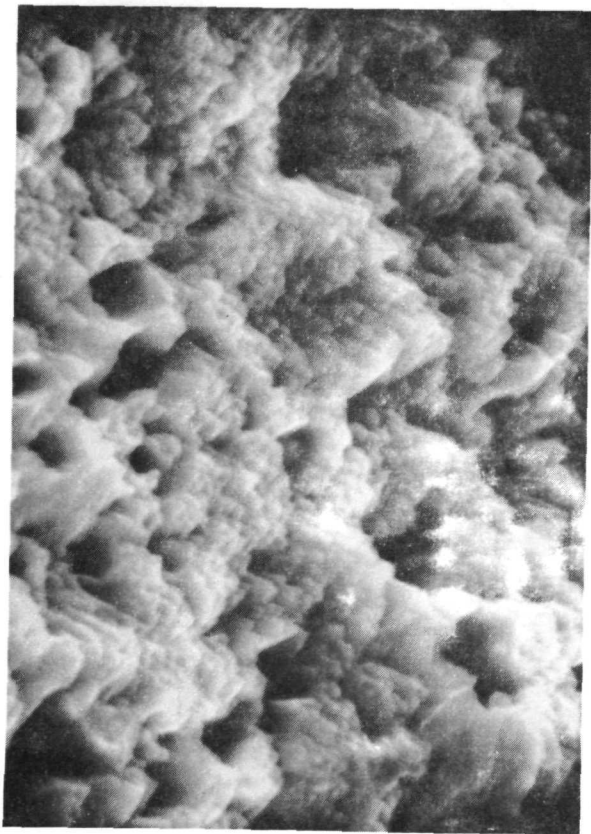
920X



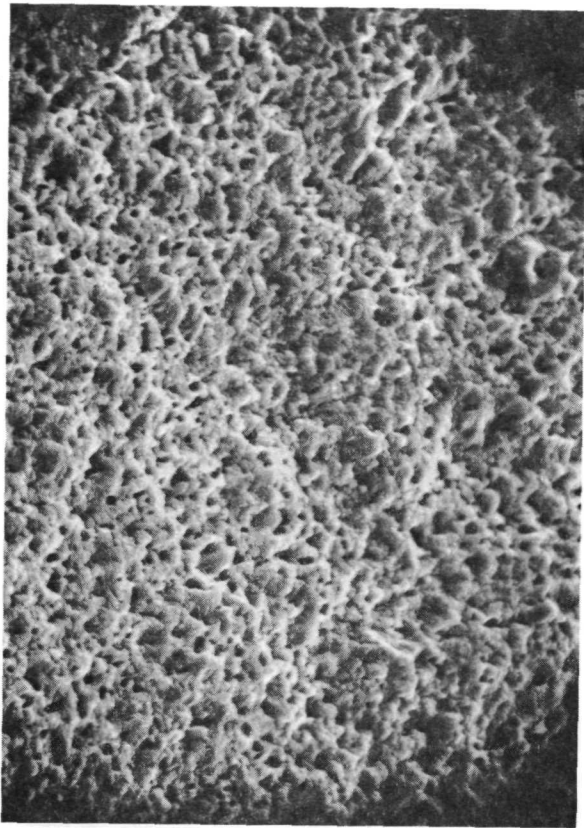
230X

Figure 26(a): SEM PHOTOGRAPHS OF UNETCHED CdS  
FILM NO. 4 OF TABLE IV

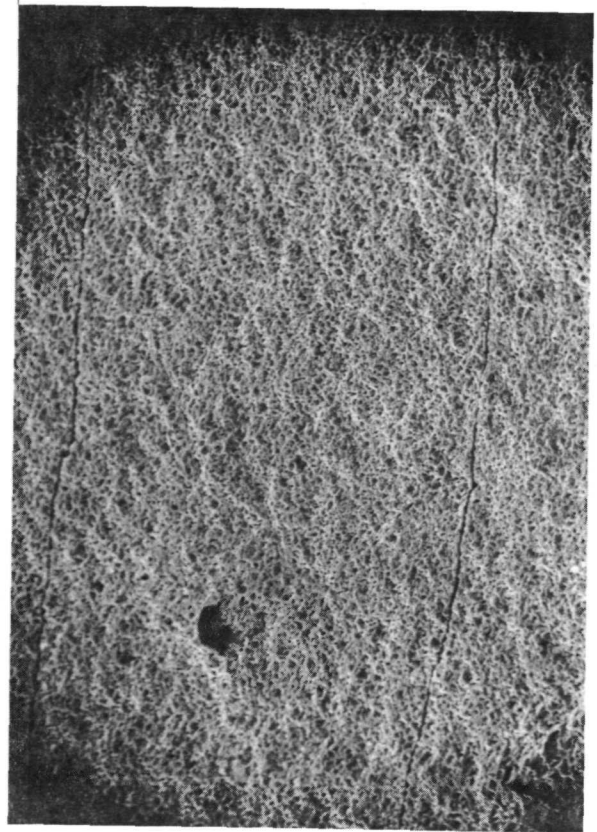




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230X

Figure 26(b): SEM PHOTOGRAPHS OF ETCHED CdS  
FILM NO. 4 OF TABLE IV

Some of the more significant observations apparent from these figures are believed to be:

1. The CdS powder preparation method did not appreciably effect the surface structure of the films (compare figures 23 and 24). [The rounded grain appearance of figure 24 was a photographic artifact.]
2. The vacuum metallized substrates produced more uniform film structures but with smaller grain sizes than the foil or plated substrates.
3. Etching the films in HCl tended to reduce the differences between substrates and caused an enormous increase in surface area. The area increase was, of course, consistent with the large increase in cell efficiency usually obtained by etching.

Etching effects on the CdS film surface structure are further exemplified in figures 27, 28, and 29 which are additional SEM photographs of CdS coated vacuum metallized kapton substrates.

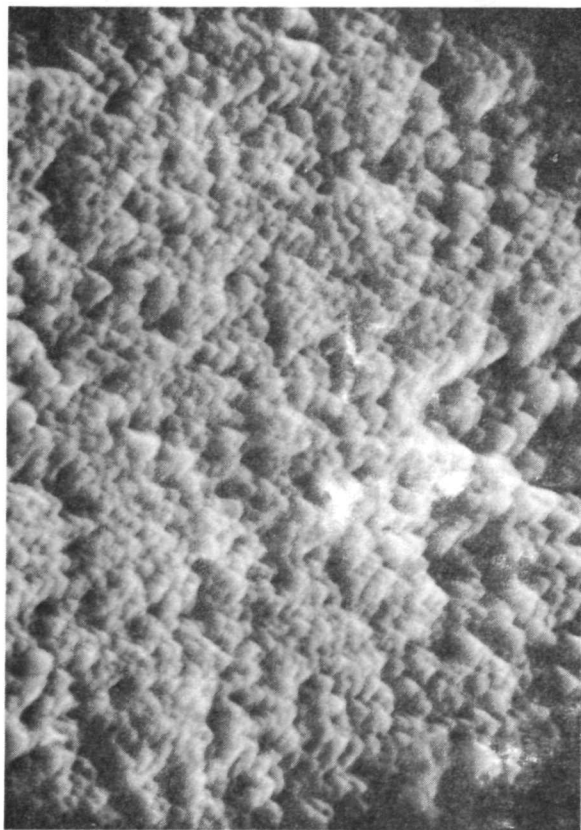
Figure 27 is the same substrates as presented in figure 23 but etched in a 47-49 percent HBr solution instead of HCl. The resulting etched structure did not seem to be influenced by the etchant--neither did the electrical properties of the cells.

Figure 28 contains a series of photographs demonstrating the effect of etch time on the CdS surface. The films were etched for 4, 6, and 8 sec. in 2:1 HCl:water at 25°C. Significant differences in surface roughness are evident between the 4 and 6 sec. films but not between the 6 and 8 sec. samples. The same was true of the measured cell performances which showed the 6 and 8 sec. etched films to be very similar and with poorer shunt characteristics than the 4 sec. cell. Furthermore, the expected increase in short circuit current with longer etching was not realized.

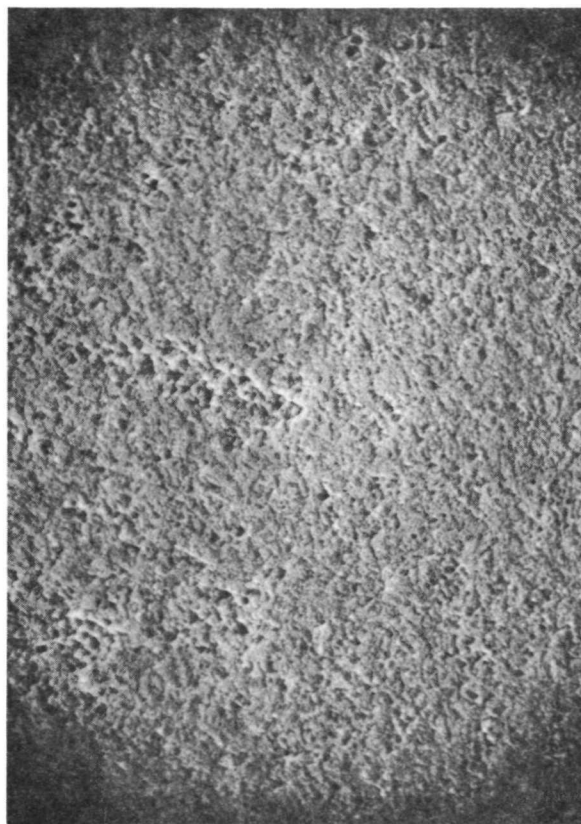
Figure 29 displays a CdS film which had been subjected to a glow discharge sputter etch. Sputter etching was briefly studied as a means for nonaqueous etching of the CdS. The substrates were attached to the cathode and sputtered for 1 minute in 50 microns of argon at 500v. As seen in this figure, holes were generated preferentially along grain boundaries---causing degradation of the cells.

#### Electrical Properties of CdS Films

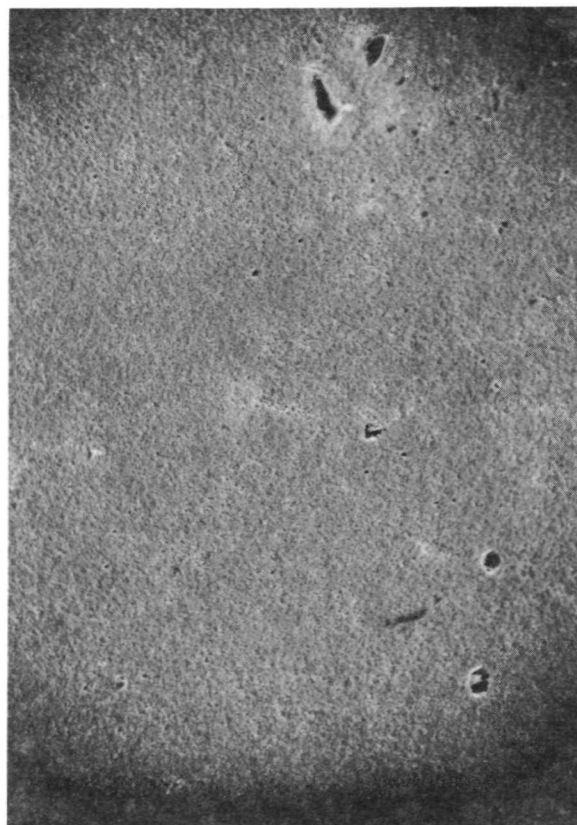
From the beginning of the cell development activity, monitoring the electrical properties of the CdS film was regarded as being an important process control condition. Consequently, a film structure suitable for making Hall and conductivity measurements was formed on each CdS deposition. The structure consisted of a typical 6-leg configuration with the sample width being 1mm and a voltage probe spacing of 5mm. The total sample length was 12mm. The substrate for this deposit was polycrystalline alumina and indium solder was used to make contact to the CdS.



4600X

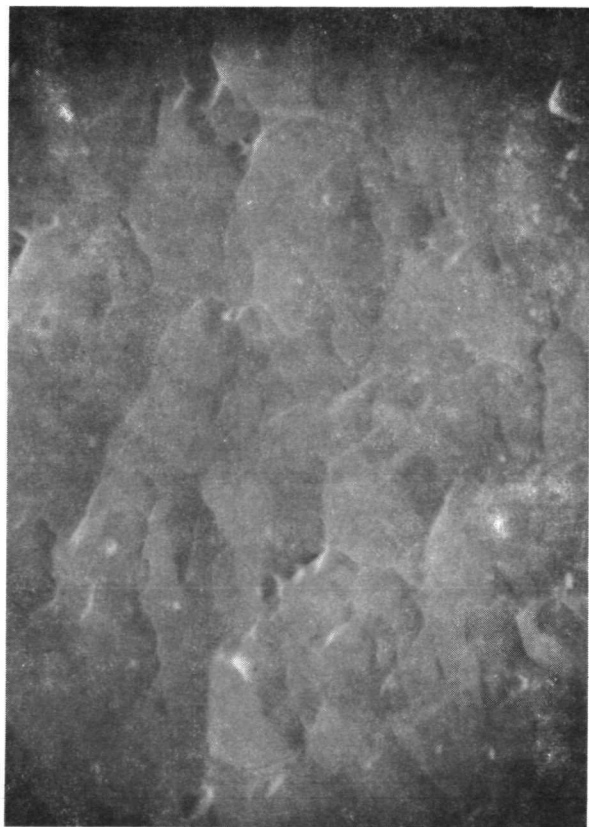


920X

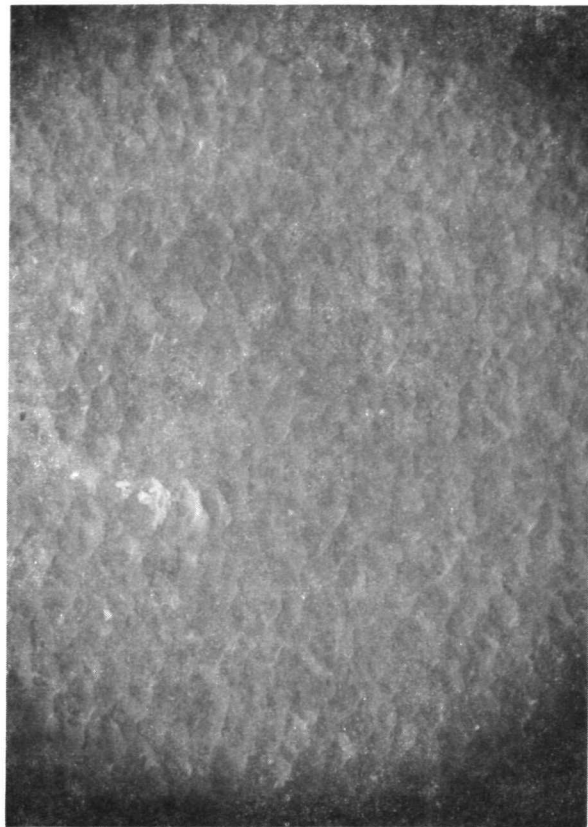


230X

Figure 27: SEM PHOTOGRAPHS OF HBr ETCHED CdS FILM NO. 1 OF TABLE IV



4600X

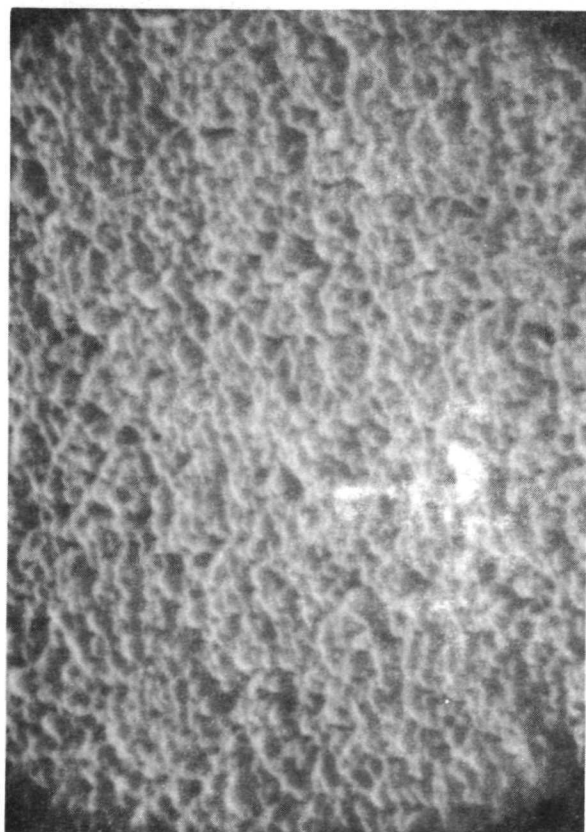


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230X

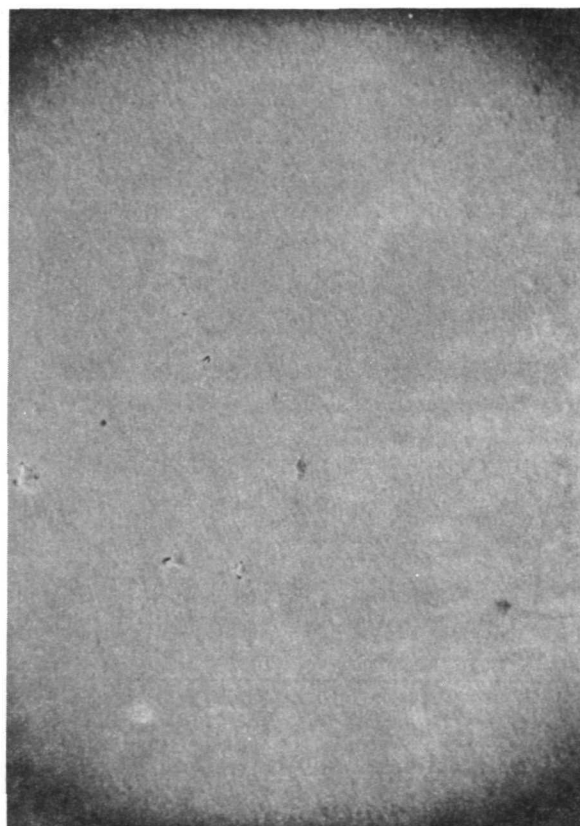
Figure 28(a): SEM PHOTOGRAPHS OF UNETCHED CdS FILM



4600X



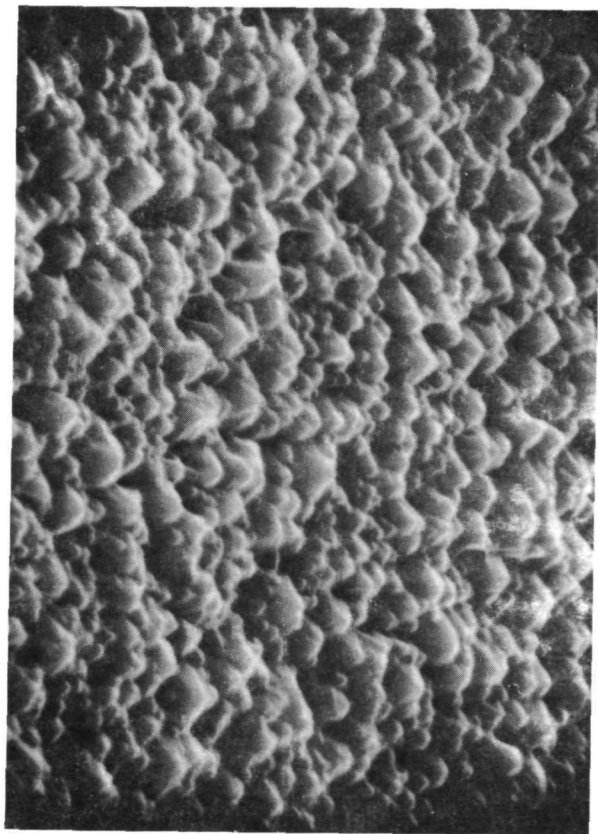
920X



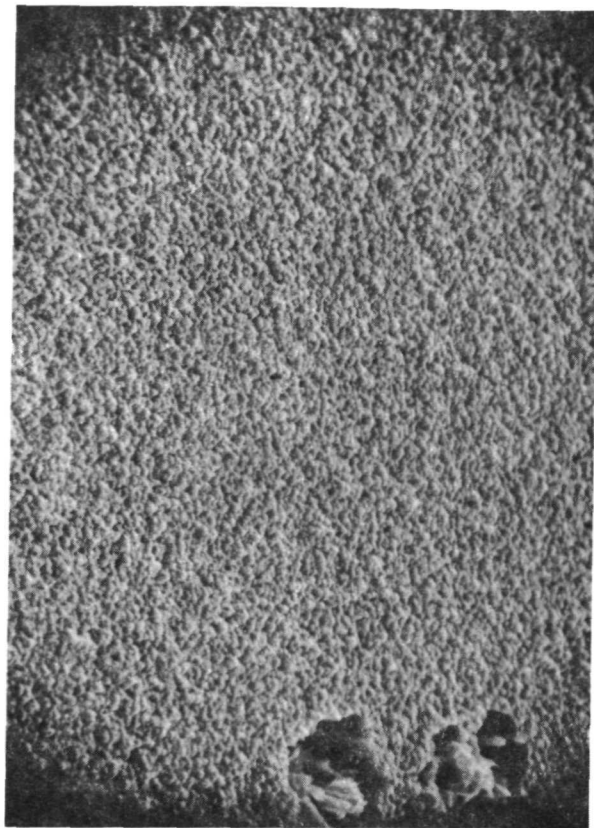
230X

Figure 28(b): SEM PHOTOGRAPHS OF CdS FILM ETCHED  
4 SEC IN HCL

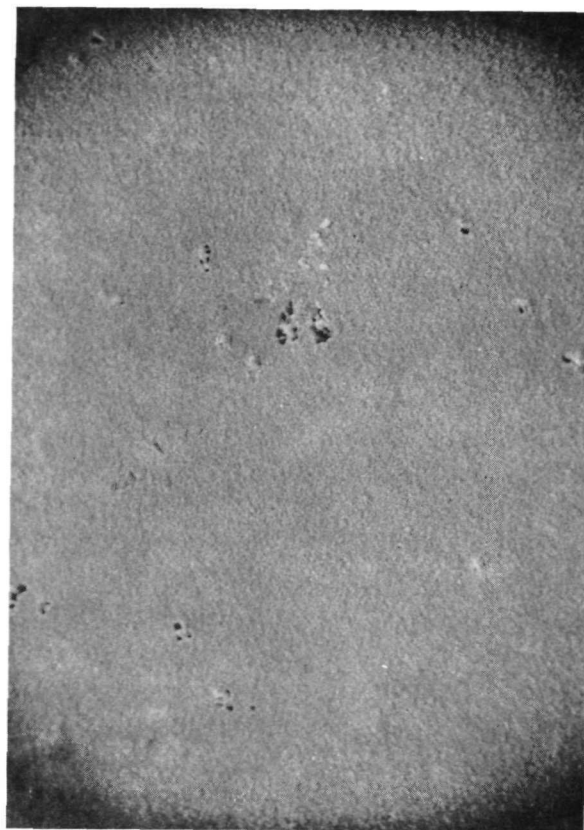




4600X

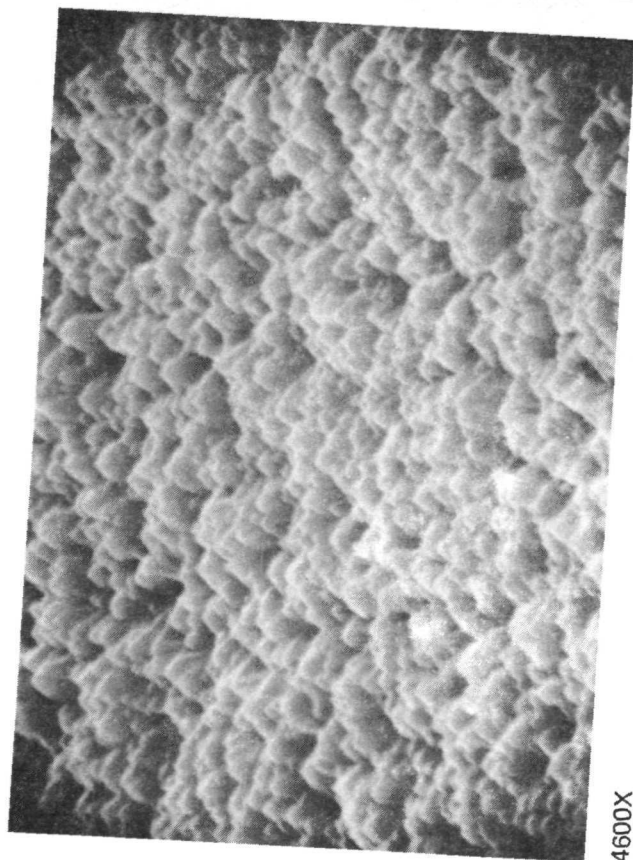


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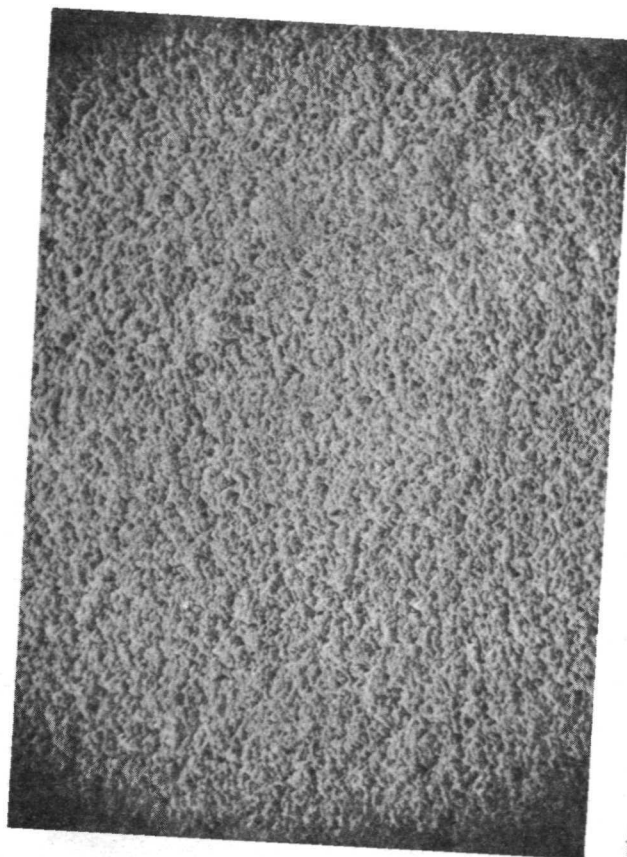


230X

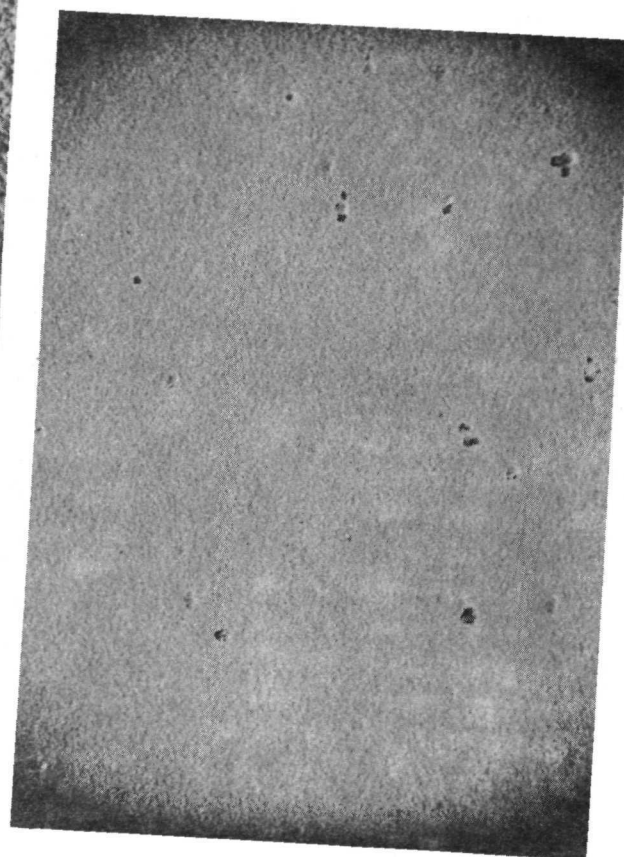
Figure 28(c): SEM PHOTOGRAPHS OF CdS FILM ETCHED  
6 SEC IN HCL



4600X

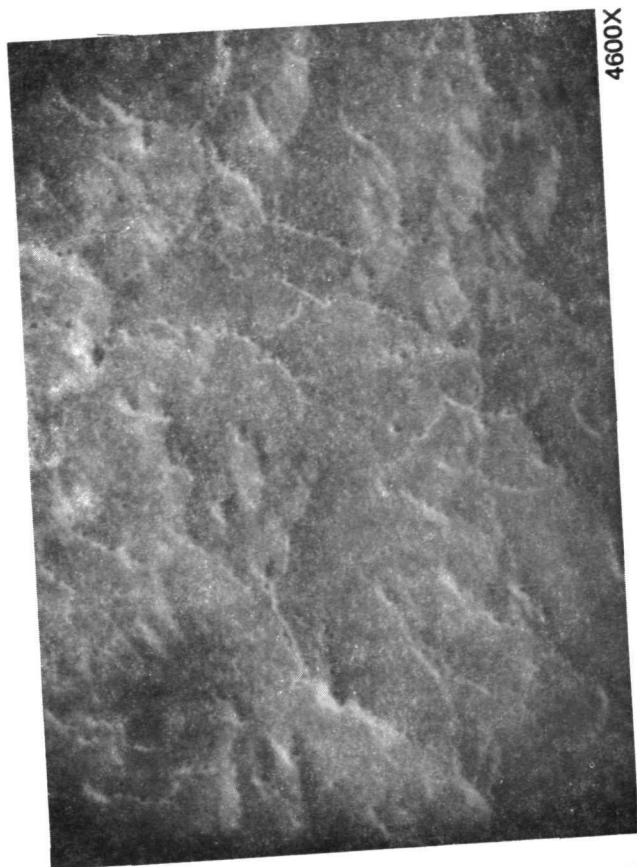


920X

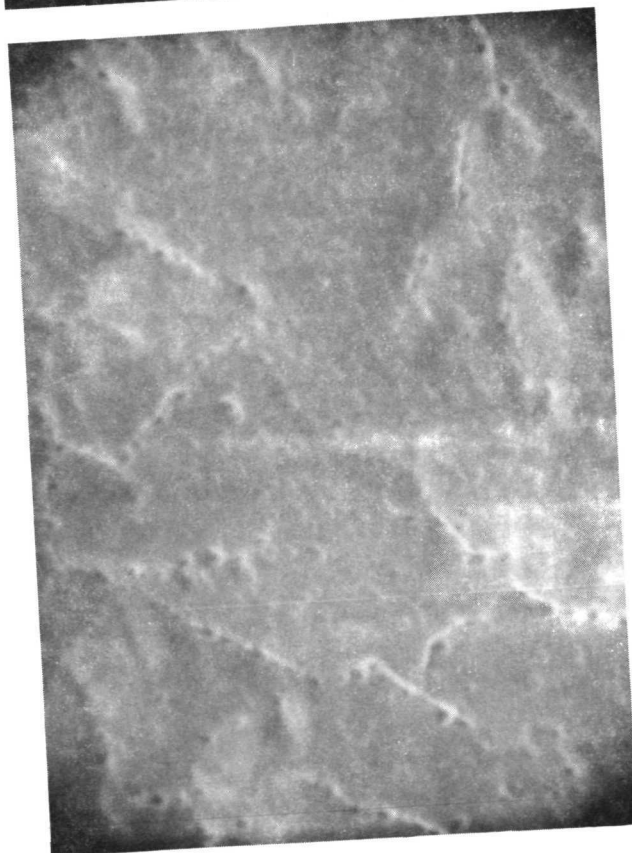


230X

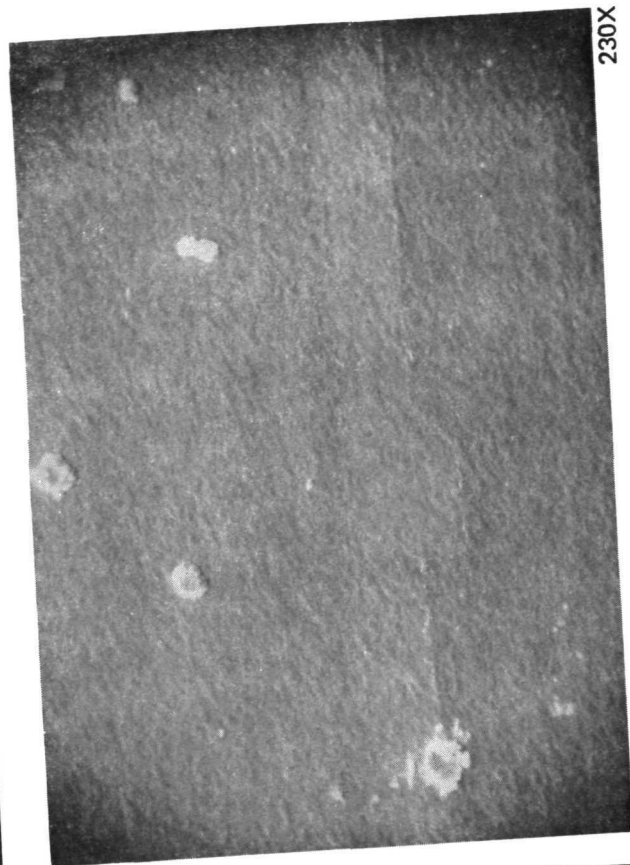
Figure 28(d): SEM PHOTOGRAPHS OF CdS FILM ETCHED  
8 SEC IN HCL



4600X



9200X



230X



920X

Figure 29: SEM PHOTOGRAPHS OF SPUTTER ETCHED CdS FILM



The test equipment used for the electrical measurements is shown in figure 30. Basically, it consists of a 9-inch Varian electromagnet with a field regulator (17 Kilogauss for these measurements), a Keithley 602 electrometer for current measurements, a Cary vibrating-reed electrometer for probe voltages and a second Cary for Hall voltage measurements. A Leeds and Northrup K-3 potentiometer was used to null out any misalignment voltage across the Hall probes in the absence of the Magnetic field.

Although the equipment was capable of testing over the temperature range from liquid nitrogen to 200°C and with or without illumination, all of the data presented in this report were obtained in the dark at room temperature.

Table V summarizes the Hall and conductivity measurements made on the CdS films deposited in the latter stage of the program.

TABLE V  
CdS FILM PROPERTIES

Film No.	Thickness (microns)	Mobility (cm <sup>2</sup> /V-sec.)	Resistivity (ohm-cm)	Carrier Concentration (cm <sup>-3</sup> )
012F1-6-71	25.9	1.3	130	3.6x10 <sup>16</sup>
012F1-12-71	38.1	2.3	6	5.0x10 <sup>17</sup>
013F1-25-71	29.7	0.7	210	4.3x10 <sup>16</sup>
013F2-23-71	21.4	0.9	48	1.4x10 <sup>17</sup>
014F2-26-71	19.2	1.2	59	8.8x10 <sup>16</sup>
014F3-12-71	19.7	1.4	250	1.8x10 <sup>16</sup>
014F3-30-71	24.7	0.9	110	6.5x10 <sup>16</sup>
016F4-22-71	17.3	0.9	150	4.6x10 <sup>16</sup>
016F4-26-71	28.0	1.0	170	3.9x10 <sup>16</sup>
016F4-29-71	26.9	2.0	200	1.6x10 <sup>16</sup>
017F5-12-71	34.5	1.4	30	1.5x10 <sup>17</sup>
017F5-14-71	31.0	0.9	87	7.9x10 <sup>16</sup>
018F5-21-71	38.6	1.0	45	1.4x10 <sup>17</sup>

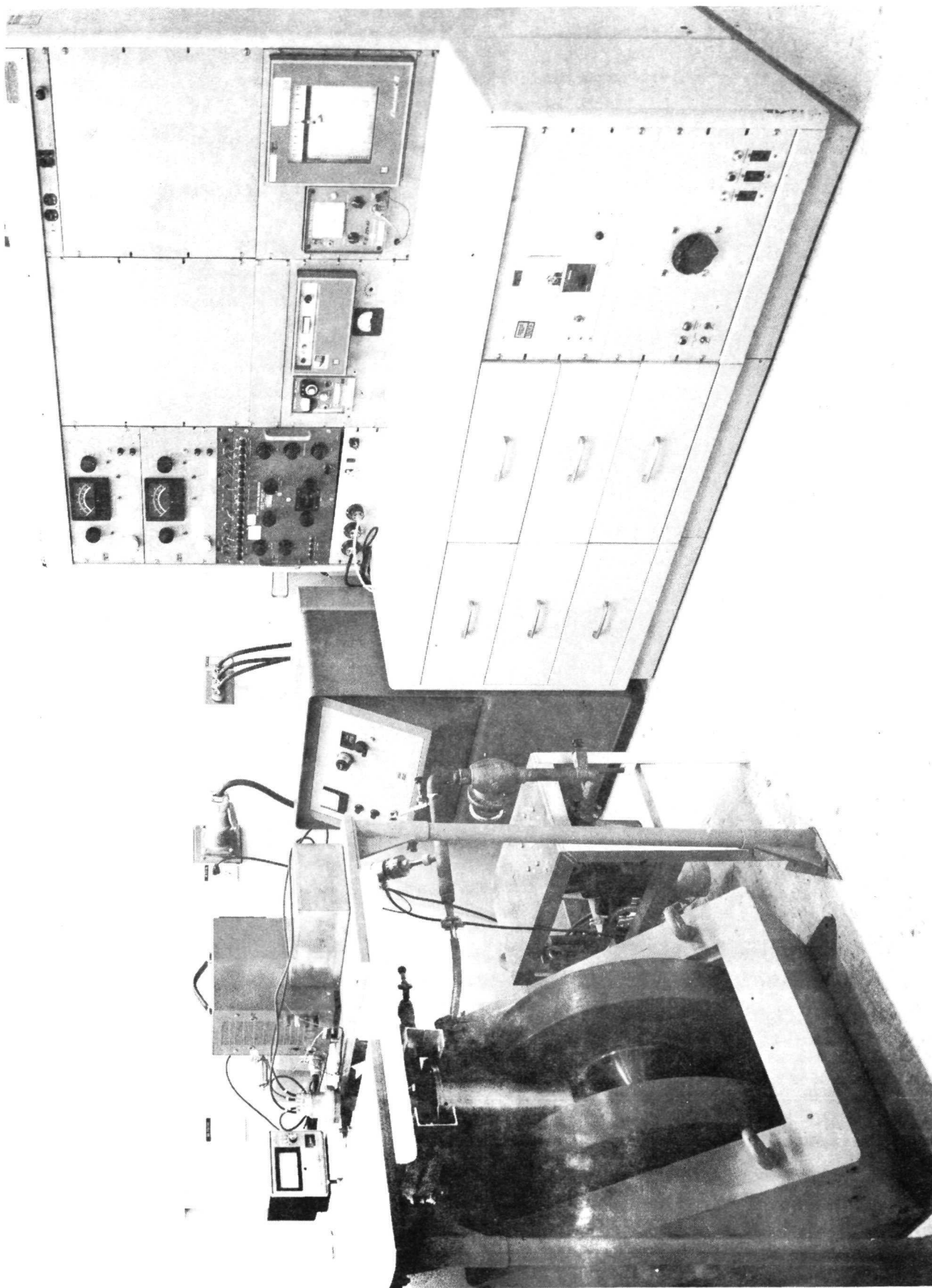


Figure 30: HALL AND CONDUCTIVITY MEASUREMENT APPARATUS

According to the data presented in this table, the CdS film properties were quite similar to those reported by others in the solar cell area. The mobilities might have been slightly lower but the conductivities and carrier concentrations were very comparable. Perhaps of greater importance is the fact that the reproducibility of film properties as indicated by this data demonstrates the degree of control over the CdS process.

### Barrier Studies

Several experimental studies on the barrier layer were conducted to acquire some knowledge concerning the dry barrier formation processes. One of these studies utilized X-ray diffraction to analyze for the crystalline structure and composition of the layer.

The first sample examined was a complete cell segment on plastic. Because of the large number of lines appearing in the diffractometer trace, analysis of the barrier layer was not readily possible. To avoid lines from noncritical cell layers, the samples were changed to the CdS films deposited onto a small (18 mm diameter) cover glass. These samples were then subjected to the same barrier formation process as had been given to the cells on plastic substrates. At first this approach failed, however, due to the stresses present in the deposited CdS film. When the barriered film was immersed in the cleaning or rinsing solutions, the CdS lost its adherence to the glass substrate. The problem was later avoided by sealing the film edges with the Sylgard encapsulant.

The substrates were then examined at three stages in the processing. These were: (1) the initial film-substrate after removal from the CdS deposition chamber; (2) after CuCl deposition and vacuum bake to form the barrier layer; and (3) after cleaning and rinsing the barriered film.

In the first trace, only the 002 and 004 lines of the highly oriented hexagonal CdS film were visible. The second trace revealed that the chemical exchange reaction had occurred, i.e., lines corresponding to the hydrated cadmium chloride ( $\text{CdCl}_2 \cdot \text{H}_2\text{O}$ ) and to the copper sulfide ( $\text{Cu}_2\text{S}$  chalcocite) were present. In addition, there were lines attributed to unreacted copper chloride ( $\text{CuCl}$ ). The third trace showed that washing in 1:5 HCl:water solution followed by rinsing removed all of the cadmium and copper chlorides--only lines corresponding to the cadmium and copper sulfides remained in the third trace. While more analysis would be necessary for positive confirmation of the existence of  $\text{Cu}_2\text{S}$  chalcocite, the strongest lines (d-values of 3.28, 2.62, 2.41 and 2.21) are consistent with this material. Moreover, the X-ray patterns from a wet barrier sample and a Clevite sample displayed the same lines.

Further support for the existence of the desired form of copper sulfide by the dry process was obtained from the optical transmission analysis of the glass substrate samples. The percent transmittance was measured over the wavelength range of 2.0 microns to 0.5 micron before and after barrier formation. Following correction for the CdS absorption, the absorption curve for the barrier layer was in excellent agreement with that presented for  $\text{Cu}_2\text{S}$  in reference 4. The curve was slightly displaced towards higher transmission which suggests a film thickness of less than the 3000Å depicted in reference 4.

This result was consistent with other studies relating to the barrier thickness. For example, according to the quartz crystal oscillator used to monitor the deposition, the CuCl film should be 2800 Å thick. For complete conversion, the Cu<sub>2</sub>S should then be approximately 1400 Å. An attempt was made to directly measure this thickness by removing the Cu<sub>2</sub>S thickness. The step was then measured with a multiple-beam interferometer. While the roughness of the KCN etched surface caused some uncertainty in the measurement, a value of 1200 Å was obtained. This thickness is seen to agree quite well with the value predicted from the CuCl thickness and that inferred by the optical transmittance spectra.

#### Glass Substrate Cells

The time required to cycle the deposition chamber in fabricating a large plastic substrate cell, was sufficiently long that it placed practical limits on the number of experiments relating to barrier formation which could be conducted. Dicing the large area cells into segments which could then be processed individually was not possible because of the methods used to interconnect the deposited grid lines for the p-contact. (This restriction was removed towards the end of the program by using silver paint or a conductive strip in the middle of the cell to interconnect the grid lines.)

A second vacuum chamber was put into service to overcome the time problem. This chamber, while smaller than the first, contained a multiple deposition fixture so that the cell deposition operations were equivalent. The cell structures were also identical excepting for width (2.5 cm vs. 15 cm). Two of these small cells were formed simultaneously on a 1-inch by 3-inch glass substrate. Since they were on glass, the substrate could be removed from its holder, processed, and then returned to the vacuum chamber for grid and other dispositions without creating serious alignment or holding problems. In addition, the rigidity of the glass eliminated the need for a backside SiO<sub>x</sub> deposition and lessened the probability of cell shorting caused by the loss of isolation strip material during cell flexure. Thus, by using glass, it was possible to more effectively concentrate on the development of cell fabrication processes without the engineering complications associated with a large area plastic substrate.

One experimental series conducted on the glass substrates pertained to the use of an evaporated film of Cu<sub>2</sub>S to form the barrier layer following the CdS deposition. The Cu<sub>2</sub>S film thickness was varied from a few hundred Angstroms to about 5500 Å. The substrate temperature was held near ambient to reduce the resistivity of the deposited Cu<sub>2</sub>S and improve film uniformity.

Very low efficiency outputs resulted from these cells even though some of the units had excellent appearing dark V-I curves. The V<sub>oc</sub> values were generally less than 250 mV and short circuit current densities in the vicinity of 1 mA/cm<sup>2</sup>.

The other major area where the glass substrate cells were applied was in the development of the dry barrier process involving the vacuum deposition of CuCl. The process variables investigated in this study were the CdS etching conditions, CuCl film thickness, and bake parameters. Glass substrate cells displaying the highest efficiencies were fabricated using a 4 sec 2:1 HCl:water etch at 25°C, 1700 Å CuCl, a 2-min vacuum bake at 180°C for barrier formation, and a 4-min air bake at 250°C following grid/silver paint interconnect application. The V-I curves for these cells are presented in figure 31 and are seen to be very similar to plastic substrate segments fabricated by like processes (see figure 15). Thus, the substrate material did not appear to have a significant effect on the basic performance of the CdS cells.

#### Junction V-I Characteristics

As part of the effort to obtain a better understanding of the junction formed by the dry barrier process, a simple circuit analysis was performed on the dark and light V-I characteristics of cell segments.

One of the samples (013F2-23-71C) analyzed was in the non-alcohol rinsed, non-etched, and vacuum deposited grid interconnect state typical of the early dry process cells. This particular segment with an area of 3.6 cm<sup>2</sup> had a V<sub>oc</sub> of 447 mv, J<sub>sc</sub> of 3.1 ma/cm<sup>2</sup>, and efficiency of 0.4 percent.

From the dark forward and reverse V-I curves the dark series (R<sub>s</sub>) and shunt (R<sub>sh</sub>) resistances were calculated to 109 ohm and 154 ohm respectively. The forward diode characteristics were then plotted, using the dark I-V curve and R<sub>s</sub>. Based on this constructed curve, a plot of log I vs. V was made to determine the two parameters I<sub>0</sub> and A in the diode equation:

$$I = I_0 \left[ \exp\left(\frac{qV}{AkT}\right) - 1 \right]$$

These were found to be I<sub>0</sub> = 1.7x10<sup>-1</sup> ma/cm<sup>2</sup> and A = 6 both were obviously too large for good device performances.

Analysis of the light I-V curve provided series and shunt resistance values of 11.6 ohm and 155 ohm respectively. While the shunt was very good, the series was far too large for efficient cell operation. What part of this resistance was due to the evaporated grid lines or to the interconnection was not known. A re-measurement of the sheet resistance of the barrier layer was conducted, however, and again found to be around 1250 ohm per square. The light generated current density, was also calculated resulting in a value of 3.9 ma/cm<sup>2</sup>.

This simple V-I analysis indicated that the light generated current in the cell was simply far too low to give high efficiency. Even if the fill factor was assumed to be 1, i.e., no internal current loss, the efficiency would only be about 1.2 percent. Thus, while the series resistance was high, the main concern at this time was redirected towards greatly improving the light generated current and not towards minimizing R<sub>s</sub>.

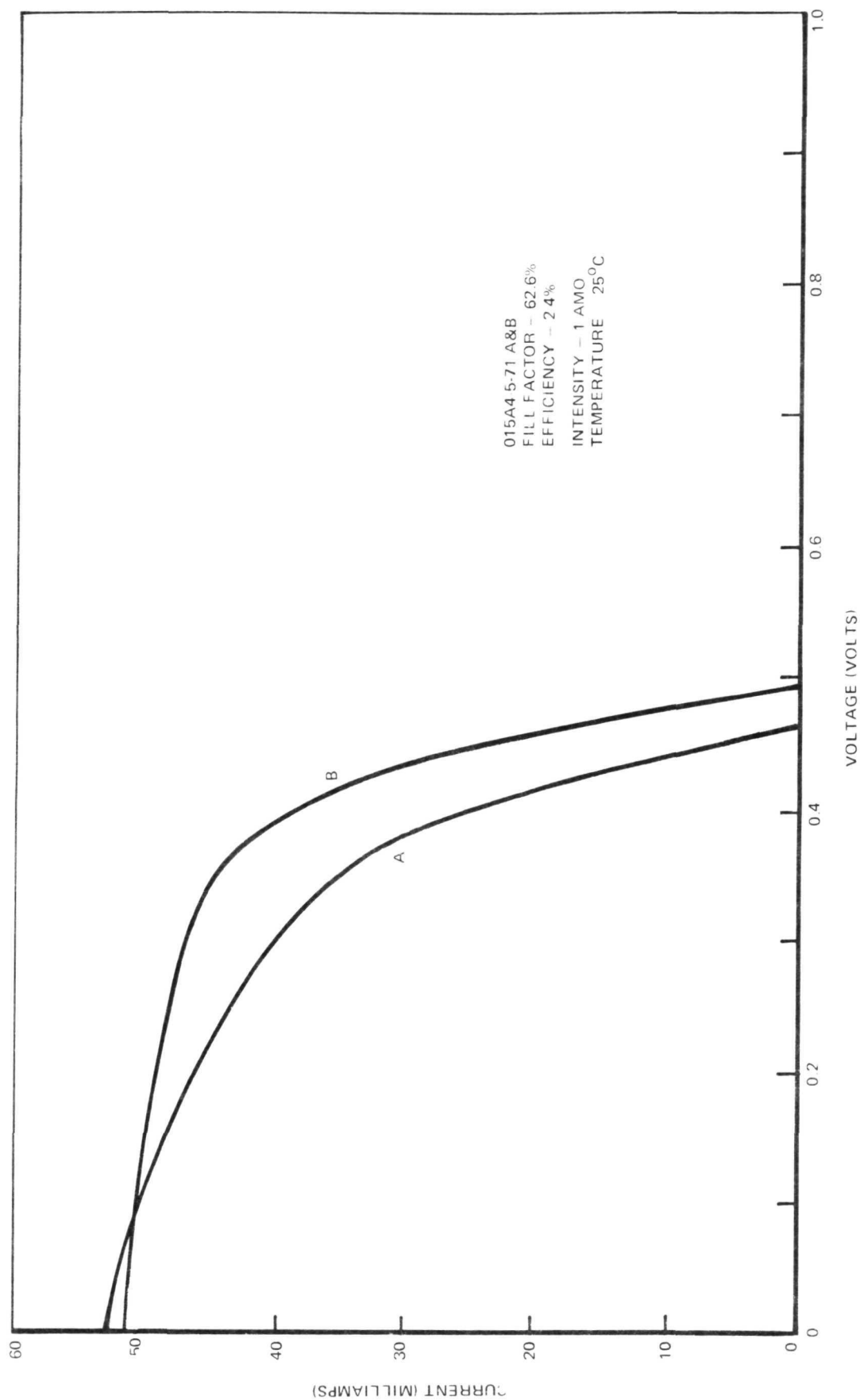


Figure 31. V-I CHARACTERISTICS OF GLASS SUBSTRATE CELLS

Following a substantial improvement in the performance of the dry barrier cells, the V-I curve analysis was repeated. Cell segment 015F3-30-71B1 was subjected to the study. This 4.0 cm<sup>2</sup> segment had been processed using an alcohol rinse 4-sec etch in 2:1 HCl:water, and interconnecting the evaporated grid lines with a silver paint bar.

The electrical characteristics of the cell were determined to be the following:

$V_{oc}$  - 508 mv;  $J_{sc}$  - 11.8 ma/cm<sup>2</sup>; efficiency - 2.7 percent;  $R_s$  dark - <10 ohm;

$R_{sh}$  dark - 500 ohm;  $R_s$  light - 1.5 ohm; and  $R_{sh}$  light - 270 ohm.

The plot of log I vs. V used to calculate the diode parameters  $I_0$  and A was found to contain two straight line sections with the break occurring at 450 mv. In the low voltage region  $I_0$  was  $1.4 \times 10^{-2}$  ma/cm<sup>2</sup> and A was 6.4, which are similar to the values for the low efficiency cell. However, at higher voltages the values were  $I_0$  -  $3.8 \times 10^{-4}$  ma/cm<sup>2</sup> and A-2.8, which are more reasonable quantities for good junction behavior. The improvements apparent in all of the above electrical parameters demonstrate the substantial advancement that had been achieved in the cell fabrication technology.

#### Electron Paramagnetic Resonance Spectroscopy

Electron Paramagnetic Resonance (EPR) measurements were taken to determine if the undesirable Cu<sup>++</sup> ion was present in the barrier or CdS layers.

Signals indicative of paramagnetic species were observed on measurements of CdS solar cells fabricated on kapton. However, it could not be readily determined whether those signals were due to the presence of Cu<sup>++</sup> or to another paramagnetic species in the solar cell. Measurements were hindered for several reasons:

(1) the metallized kapton contained paramagnetic species or contamination which masked the presence of the Cu<sup>++</sup> signal. The signal strength from these contaminants varied from sample to sample, (2) the presence of metallized layers on the kapton substrate absorbed the microwave power in the EPR cavity, resulting in reduced sensitivity in the system. For these reasons samples of CdS on borosilicate glass disks were prepared. EPR analysis of these samples showed no signal which could be correlated with a paramagnetic species. A barriered CdS sample was also analyzed and no paramagnetic species signal was seen.

The EPR study was concluded after an unsuccessful attempt to convert some of the Cu<sub>2</sub>S to CuS using the techniques suggested in Ref. 4. If the Cu<sub>2</sub>S could have been oxidized to form cupric ions, it would then have been possible to determine whether Cu<sup>++</sup> in a Cu<sub>2</sub>S-CdS matrix could in fact be measured using EPR.

Because of the negative results in forming the meaningful calibration sample for the EPR analysis, the actual value of the technique relating to solar cells remains in question. None of the test results indicate, however, a high potential for the method.



## Reactive Evaporation of CdS

An undesirable feature of the cell fabrication process common to this laboratory and nearly all others, involves the requirement for CdS deposition at elevated temperatures---about 200°C. Kapton, the most frequently used substrate material, has a substantially higher thermal expansion coefficient than CdS. The substrate curl resulting from the mismatch in coefficients greatly complicates the cell fabrication---especially when the fabrication process requires other film depositions as described in this report. Consequently, a low temperature method of CdS deposition should have appreciable importance.

With this concept in mind, a brief series of experiments was conducted using a reactive evaporation technique, i.e., evaporation of the CdS in H<sub>2</sub>S environment. Film samples were deposited onto glass substrates according to the deposition parameters listed in table VI.

TABLE VI

REACTIVE EVAPORATION OF CdS in H<sub>2</sub>S

Sample No.	Thickness (Å)	Rate (Å/Sec)	Substrate Temperature (°C)	H <sub>2</sub> S Pressure (Torr)	Mobility (cm <sup>2</sup> V-sec)	Resistivity (ohm-cm)	Carrier Concentration (cm <sup>-3</sup> )
013S1-27-71B	11,000	17	100	none	6.9	37	2.4x10 <sup>15</sup>
013S1-28-71	11,000	16	100	5x10 <sup>-5</sup>	11.2	950	6.2x10 <sup>14</sup>
013S2-2-71	11,000	6	100	5x10 <sup>-5</sup>	4.6	2600	4.7x10 <sup>14</sup>

The films were deposited through masks such that a Hall structure, optical absorption area, and film thickness area were formed. As can be seen from the electrical properties listed in Table VI, a definite reaction can be realized by the H<sub>2</sub>S reactive evaporation technique. This conclusion was further supported by the optical absorption spectra which showed the films deposited in H<sub>2</sub>S had steeper absorption edges and were more transparent at the longer wavelengths.

Both the optical and electrical properties can be explained in terms of an improved film stoichiometry with the H<sub>2</sub>S. No differences in the physical structure of films deposited with or without H<sub>2</sub>S was evident from a SEM analysis.

While additional work is obviously necessary, these initial results indicate that it may be feasible to deposit the CdS at lower substrate temperatures without producing films with unacceptable stoichiometry for solar cell applications.



## CELL TEST AND FABRICATION DATA

Table VII shows the electrical characteristics of submodules fabricated by the dry barrier technique for which data was obtained at 25°C and 60°C. These cells were not shorted after complete processing and were not segmented for parametric process studies. The calculated temperature coefficients for the cells are listed in Table VIII. Electrical characteristics of modules obtained only at 25°C are shown in Table IX. These submodules were the last group fabricated.

The fabrication parameters for the modules contained in these tables are summarized in Table X.

A more detailed description of the processes and equipment used in this program is contained in a separate document of drawings and process specifications.

TABLE VII: CHARACTERISTICS OF CELLS AT 25°C AND 60°C

SUBMODULE NO	CELL	OPEN CIRCUIT VOLTAGE-VOLTS		SHORT CIRCUIT CURRENT-mA		MAXIMUM POWER-mW		VOLTAGE AT MAX. POWER-V		CURRENT AT MAX. POWER-mA		FILL FACTOR PER CENT		CONVERSION EFFICIENCY PER CENT	
		25	60	25	60	25	60	25	60	25	60	25	60	25	60
013F2-9-71	A	0.447	0.404	93	78	15.5	11.1	0.282	0.221	55	50	37.3	35.2	39	0.28
	B	0.423	0.384	141	136	20.7	19.0	0.243	0.220	85	82	40.0	34.5	52	0.45
	C														
013F2-12-71	A	0.381	0.390	137	99	14.6	11.5	0.200	0.210	73	55	38.3	29.8	33	0.26
	B	0.460	0.418	120	84	16.1	9.6	0.244	0.228	42	41.7	27.4	37	0.22	
	C	0.424	0.341	136	99	17.4	9.1	0.223	0.194	78	47	38.6	27.0	40	0.21
013F2-23-71	A	0.379		47		5.1		0.210		24.5		28.6		12	
	B	0.441		129		25.0		0.290		86		43.9		60	
	C	0.440		66		8.4		0.230		36.5		28.9		20	
013F2-26-71	A	0.405	0.383	57	46	8.3	6.3	0.244	0.226	34	28	36.0	35.8	23	0.17
	B	0.330	0.282	58	44	6.0	4.2	0.187	0.170	32	24.5	34.4	33.9	17	0.12
	C	0.245	0.190	80	63	6.8	3.9	0.141	0.100	48	38.5	34.7	32.6	19	0.11
0143F3-10-71	A	0.428	0.365	66.4	51.5	8.46	5.24	0.235	0.193	36.8	27.3	29.0	27.0	20	0.125
	B	0.273	0.183	29.17	13.2	2.06	0.62	0.137	0.095	15.0	6.5	25.5	25.7	03	0.015
	C	0.240	0.144	13.3	7.3	0.62	0.26	0.117	0.080	7.0	3.3	25.7	25.1	02	0.086
014F3-12-71	A	0.428	0.383	7.1	27.2	6.0	3.09	0.228	0.210	26.6	14.7	29.9			
	B	0.439	0.377	9.8	8.7	1.3	0.94	0.252	0.200	5.1	4.7	30.5			
	C														
014F3-17-41	A	0.146	0.375	28.5	21.6	3.04	0.206								
	B														
	C	0.419	0.357	70.2	51.0	8.58	5.04	0.223		38.5	27.2	25.2		0.204	

TABLE VIII: TEMPERATURE COEFFICIENTS OF CELLS BETWEEN 25°C AND 60°C

SUBMODULE NO.	CELL	OPEN-CIRCUIT VOLTAGE V/°C	SHORT-CIRCUIT CURRENT mA/°C	MAXIMUM POWER mW/°C
013F 2-9-71	A			
	B	- 0.0012	- 0.43	- 0.13
	C	- 0.0011	- 0.14	- 0.68
013F 2-12-71	A	0.0003	- 1.09	- 0.09
	B	- 0.0012	- 1.03	- 0.19
	C	- 0.0024	- 1.00	- 0.24
013F 2-26-71	A	- 0.0006	- 0.31	- 0.06
	B	- 0.0014		- 0.05
	C	- 0.0016	- 0.26	- 0.08
014F 3-10-71	A	- 0.0018	- 0.43	- 0.09
	B	- 0.0026	- 0.45	- 0.04
	C	- 0.0027	- 0.17	- 0.02
014F 3-12-71	A	- 0.0013	- 0.57	- 0.08
	B	- 0.0018	- 0.03	- 0.01
	C			
014F 3-24-71	A	- 0.0012	- 0.20	- 0.03
	B			
	C	- 0.0012	- 0.55	- 0.10

TABLE IX: CHARACTERISTICS OF CELLS AT 25°C

SUBMODULE NO.	CELL	OPEN CIRCUIT VOLTAGE-VOLTS	SHORT CIRCUIT CURRENT-mA	MAXIMUM POWER-mW	VOLTAGE AT MAX. POWER-V	CURRENT MAX. POWER-mA	FILL FACTOR PERCENT	CONVERSION EFFICIENCY PERCENT
019F6-9-71	A	0.425	178	24.6	0.251	98	32.5	0.61
	B	0.432	179	25.9	0.252	103	33.6	0.64
	C	0.414	163	21.8	0.248	88	32.4	0.55
019F6-11-71	A	0.424	114	13.6	0.211	64.5	28.1	0.34
	B	0.440	152	18.0	0.228	79	27.9	0.45
	C	0.450	163	20.8	0.236	88	28.3	0.52
019F6-15-71	A	0.402	206	26.9	0.240	112	32.4	0.67
	B	0.425	200	28.7	0.252	114	33.8	0.71
	C	0.398	157	19.1	0.233	82	30.6	0.47
019F6-18-71	A	0.399	198	25.6	0.239	107	32.4	0.64
	B	0.432	210	29.0	0.242	120	32.0	0.72
	C	0.392	205	24.5	0.217	113	30.5	0.61
019F6-22-71	A	0.392	151	26.0	0.280	93	35.1	0.65
	B	0.448	113	17.7	0.256	69	34.9	0.44
	C	0.488	134	22.4	0.273	82	34.3	0.56
019F6-25-71	A	0.390	176	22.1	0.228	97	32.2	0.55
	B	0.394	153	19.5	0.226	86	32.3	0.48
	C	0.325	153	14.5	0.169	86	29.0	0.36



## SUMMARY OF RESULTS

The technology of integrated electronic circuits was applied to the design and fabrication of modules of interconnected CdS thin-film solar cells. The feasibility of this approach was demonstrated by developing operational single cells and submodules (3 series connected single cells) based upon the integrated circuit concepts.

Front wall cell structures were formed using through-mask vacuum-deposited thin films on both copper clad and plain (subsequently vacuum metallized with copper) 1-mil thick kapton substrates. The selection of the plain kapton was favored because of the easier cell deposition processes and improved uniformity/reproducibility of surface characteristics.

An acceptable metallization for the kapton substrates was formed as a sandwich of three vacuum-deposited metal films. The first layer was a 450 Å layer of nichrome that adhered strongly to the kapton and served as a good base for subsequent metallizations. The second layer was a 1-2 micron copper film that possessed a high electrical conductivity and relative chemical inertness to the solutions used in cell processing. The third layer was a 500 Å film of chromium that was found to promote an ohmic contact and very high adherence for the thick (approximately 1 mil) vacuum-deposited CdS film.

$\text{SiO}_x$  films of about 10 microns thickness deposited on the back surface of the kapton substrate increased the substrate rigidity sufficiently to prevent the usual curling caused by the thick CdS film deposition.

CdS film spray outside of the area defined by the deposition masks was controlled by a combination of proper mask design and deposition procedure/equipment. The achievement of minimal spray was essential to the demonstration of feasibility for the cell interconnection concepts.

Photovoltaic barriers of copper sulfide were formed on the deposited CdS films either by wet process or by a vacuum deposition (dry) process. In the wet process, the substrates were immersed in a 90°C aqueous solution containing NaCl, HCl, and saturated with CuCl. The dry process barrier was formed by depositing 1100 Å to 1700 Å of CuCl onto the CdS followed by a low-temperature bake in hydrogen. The electrical characteristics of the dry process cells were found to be superior in terms of short circuit current density, open circuit voltage, and conversion efficiency. The most efficient cell segment displayed values of 11.8 ma/cm<sup>2</sup>, 508 mv, and 2.7 percent respectively for these parameters. Spectral response of the segment was peaked at 0.62 microns and contained a significant red contribution. X-ray and optical absorption data further confirmed that the barrier layer was Cu<sub>2</sub>S.

To obtain high conversion efficiencies it was necessary to clean the CdS films in alcohol or carbon disulfide, etch in HCl, and then rinse in DI water.

No strong influence of substrate material was detected as cells of approximately the same area fabricated on glass and kapton exhibited essentially identical characteristics.

A 3-5000 Å vacuum deposited SiO<sub>2</sub> thin film was shown to be effective in masking the edges of the CdS film from <sup>x</sup>etchants and barrier formation processes, but was not adequate for electrical isolation between interconnect and substrate metallization layers. A silicone (Sylgard 186) applied by silk screening was successfully used for an isolation layer.

It was found feasible to make the p-contact to cell/module structures with deposited Cr/Au thin films. A Cr (500 Å)/Au(5000 Å) film combination served both for the grid lines on top of the barrier layer and for interconnecting cells into modules.

A cell passivation procedure was developed based upon a highly transparent layer of silicone R63-488, brushed onto the cell surface and then cured.

A number of analytical studies were conducted relating to the material properties of the CdS and barrier layer. The scanning electron microscope, Hall effect, and electrical conductivity were found to be of value in these studies while little meaningful data was obtained using electron paramagnetic resonance spectroscopy.

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